EM79F701N

8-BIT Microcontroller

Product Specification

DOC. VERSION 1.2

ELAN MICROELECTRONICS CORP.

Dec. 2024

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ELAN MICROELECTRONICS CORPORATION

Headquarters:
Address: No. 12, Innovation 1st Rd., Hsinchu Science Park, Hsinchu 300092, Taiwan (R.O.C.)
Tel: +886 3 563-9977
Fax:+886 3 563-9966
webmaster@emc.com.tw
http://www.emc.com.tw

Hong Kong:
Elan (HK) Microelectronics Corporation, Ltd.
Address: Flat A, 19/F., World Tech Centre, 95 How Ming Street, Kwun Tong, Kowloon, Hong Kong.
Tel: +852 2723-3376
Fax:+852 2723-7780

USA:
Elan Information Technology Group (U.S.A.)
Address: 10268 Bandley Drive Suite 101 , Cupertino , CA 95014,USA
Tel: +1 408 366-8225
Fax:+1 408 366-8225

Shenzhen:
Elan Microelectronics Shenzhen, Ltd.
Address: 8A Floor, Microprofit Building, Gaoxin South Road 6, Shenzhen Hi-Tech Industrial Park, South Area, Shenzhen, China 518057
Tel: +86 755 2601-0565
elan-sz@elanic.com.cn

Shanghai:
Elan Microelectronics Shanghai, Ltd.
Address: Room 703, No. 3, Lane88, Shengrong Road, Pudong New Area, Shanghai, China 201203
Tel :+ 86 21-50803866
elan-sh@elanic.com.cn

Contents

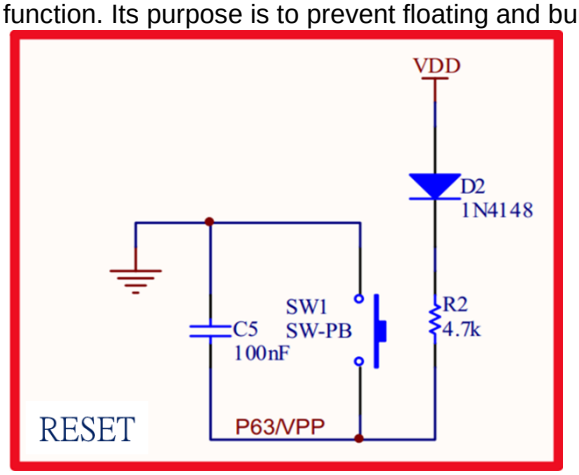
Specification Revision History

Version	Revision Description	Date
1.0	Released version	2023.08.17
1.1	Add EM79F701NMS10	2023.12.06
1.2	1. Modify R5, R6 initialized value to 1 after /RESET and WDT. 2. Modify SR bit 4 T initialized value to unknown after Power On.	2024.12.13

User Application Note

(Before using this chip, take a look at the following description note, it includes important messages.)

1. When programming EM79F701N, Writer will supply 5V to VDD and supply max 11.2V to VPP (RESET PIN). Therefore, during EM79F701N programming, pay attention to the voltage rating of the surrounding components.
2. We strongly recommend that you place the following circuits on the reset pin, regardless of pin function. Its purpose is to prevent floating and burning when the high voltage backflush.



3. The priority of TS is higher than IOC62. Thus, P62 is set as TCC external clock source in default. If you want to set P62 as output pin, you have to clear TS bit in advance.
4. After LVDEN bit is set, you must wait at least 40us to stabilize LVD. If you go to sleep immediately after setting LVDEN, LVD will not work normally.
5. Port 5 and Port 6 I/O state will be initialized as 1 after a reset. Hence, assign I/O state before configure I/O as output is suggested to prevent unexpected output state appearing after a reset occurs. Refer to Section 6.4, I/O Ports for further details.
6. After a power-on reset, the Time-out bit T is unknown. To implement different initialization procedures, it is recommended to check the value of P flag at the beginning of the program. Refer to Section 6.5.4 for further details.

1 General Description

The EM79F701N is an 8-bit microprocessor designed and developed with low-power and high-speed CMOS technology. It has an on-chip 1k×16-bit programmable ROM.

With its enhanced Flash-ROM features, the EM79F701N provides a convenient way of developing and verifying user's programs. Moreover, this Flash device offers the advantages of easy and effective program updates, using development and programming tools. User can avail of the ELAN Writer to easily program your development code.

2 Features

- CPU Configuration
  - 1k × 16 bits on-chip program ROM
    *Endurance: 10,000 cycles at 25°C
  - 48 × 8 bits on-chip registers (SRAM, General purpose)
  - 5-level stacks for subroutine nesting
  - Typically 3mA at 5V/4 MHz
  - Typically 20μA at 3V/32kHz
  - Typically 1μA during Sleep mode
- I/O Port Configuration
  - 2 bidirectional I/O ports : P5, P6
  - 12 I/O pins
  - Wake-up port : P6
  - 7 programmable pull-down I/O pins
  - 7 programmable pull-high I/O pins
  - 7 programmable open-drain I/O pins
  - External interrupt with wake-up: P60
- Operating Voltage Range:
  - 2.1V ~ 5.5V at 0 ~ 70°C (Commercial)
  - 2.3V ~ 5.5V at -40 ~ 85°C (Industrial)
- Operating frequency range (base on two clocks):
  - IRC mode:

Internal RC Frequency	Drift Rate (NUWTR)			
	Temperature (-40°C~85°C)	Voltage	Process	Total
4 MHz	±2.5%	±3% ***(2.1~5.5V)**	±0.5%	±6%
16 MHz	±2.5%	±2% ***(4.0~5.5V)**	±0.5%	±5%
8 MHz	±2.5%	±2% ***(3.0~5.5V)**	±0.5%	±5%
1 MHz	±2.5%	±3% ***(2.1~5.5V)**	±0.5%	±6%

* Operating voltage range

Internal RC Frequency	Drift Rate (UWTR)			
	Temperature (-40°C~85°C)	Voltage	Process	Total
4 MHz	±2.5%	±3% ***(2.1~5.5V)**	±1.5%	±7%
16 MHz	±2.5%	±2% ***(4.0~5.5V)**	±1.5%	±6%
8 MHz	±2.5%	±2% ***(3.0~5.5V)**	±1.5%	±6%
1 MHz	±2.5%	±3% ***(2.1~5.5V)**	±1.5%	±7%

  - Crystal mode:
    DC ~ 20MHz / 2clks @ 5V
    DC ~ 8MHz / 2clks @ 3V
    DC ~ 4MHz / 2clks @ 2.1V
- Peripheral Configuration
  - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - External interrupt input pin
  - Power-on reset (POR:1.8V) and 3 programmable level voltage reset (LVR: 4.0, 3.5, 2.7V)
  - 4 programmable level voltage detector
    LVD : 4.5, 4.0, 3.3, 2.2V
  - 2/4 clocks per instruction cycle selected by code option
  - Power down (Sleep) mode
  - High EFT immunity
- Four Available Interrupts:
  - TCC overflow interrupt
  - Input-port status changed interrupt
  - External interrupt
  - Low voltage detect interrupt
- Special features
  - Programmable free running watchdog timer
  - Power saving sleep mode
  - Selectable oscillation mode
  - Programmable prescaler of oscillator set-up time
- Package Type
  - 14-pin DIP 300mil : EM79F701ND14
  - 14-pin SOP 150mil : EM79F701NSO14
  - 10-pin MSOP 118mil : EM79F701NMS10

Note: *These are all Green products which do not contain hazardous substances.*

3 Pin Configuration

(1) EM79F701N 14-Pin DIP/SOP

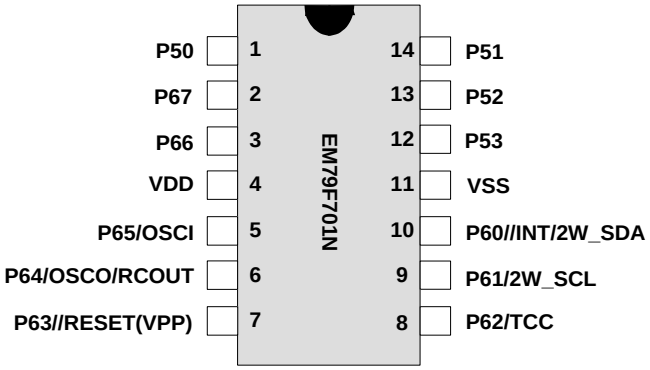


Figure 3-1 EM79F701ND14 / SO14

(2) ***EM79F701N 10-Pin MSOP***

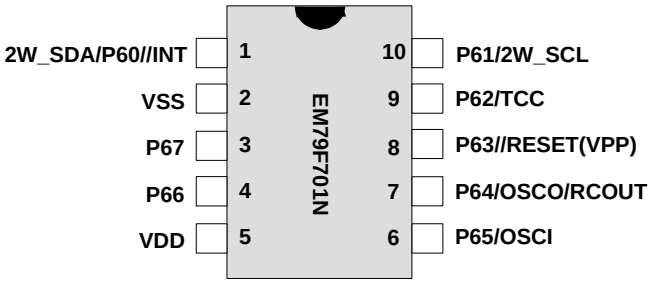


Figure 3-2 EM79F701NMS10

4 Pin Description

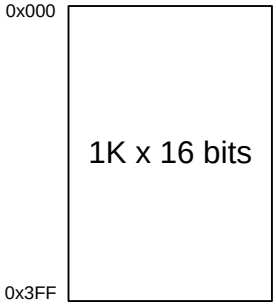
Name	Function	Input Type	Output Type	Description
P50~P52	P50~P52	ST	CMOS	Bidirectional I/O pin with programmable pull-down.
P53	P53	ST	CMOS	Bidirectional I/O pin
P60//INT/2W_SDA	P60	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high and pin change wake-up.
	/INT	ST	–	External interrupt pin
	2W_SDA	ST	CMOS	On Chip Program data pin
P61/2W_SCL	P61	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high and pin change wake-up.
	2W_SCL	ST	–	On Chip Program clock pin
P62/TCC	P62	ST	CMOS	Bidirectional I/O pin with programmable pull-down, open-drain, pull-high and pin change wake-up.
	TCC	ST	–	Real Time Clock/Counter clock input (default)
P63//RESET (VPP)	P63	ST	CMOS	Bidirectional I/O pin with programmable pull-down and pin change wake-up. (open-drain)
	/RESET	ST	–	External pull-high reset pin
	VPP	Power	–	VPP pin for programming (10.8V~11.2V)
P64/OSCO/RCOUT	P64	ST	CMOS	Bidirectional I/O pin with programmable open-drain, pull-high and pin change wake-up.
	OSCO	–	XTAL	Clock output of crystal/ resonator oscillator
	RCOUT	–	CMOS	Clock output of internal RC oscillator
P65/OSCI	P65	ST	CMOS	Bidirectional I/O pin with programmable open-drain, pull-high and pin change wake-up
	OSCI	XTAL	–	Clock input of crystal/resonator oscillator
P66~P67	P66~P67	ST	CMOS	Bidirectional I/O pin with programmable open-drain, pull-high and pin change wake-up
VDD	VDD	Power	–	Power (4.5V~5.5V when programming)
VSS	VSS	Power	–	Ground

Legend: *ST: Schmitt Trigger input* *CMOS: CMOS output*
AN: analog pin *XTAL: oscillation pin for crystal / resonator*

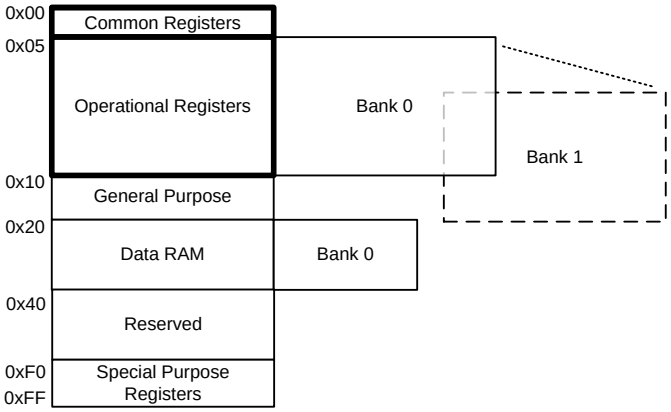
5 System Overview

5.1 Memory Map

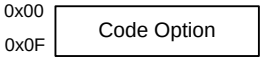
User Program Area



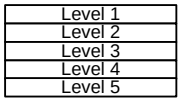
Registers and Data RAM Memory



Option Area



STACK



5.2 Functional Block Diagram

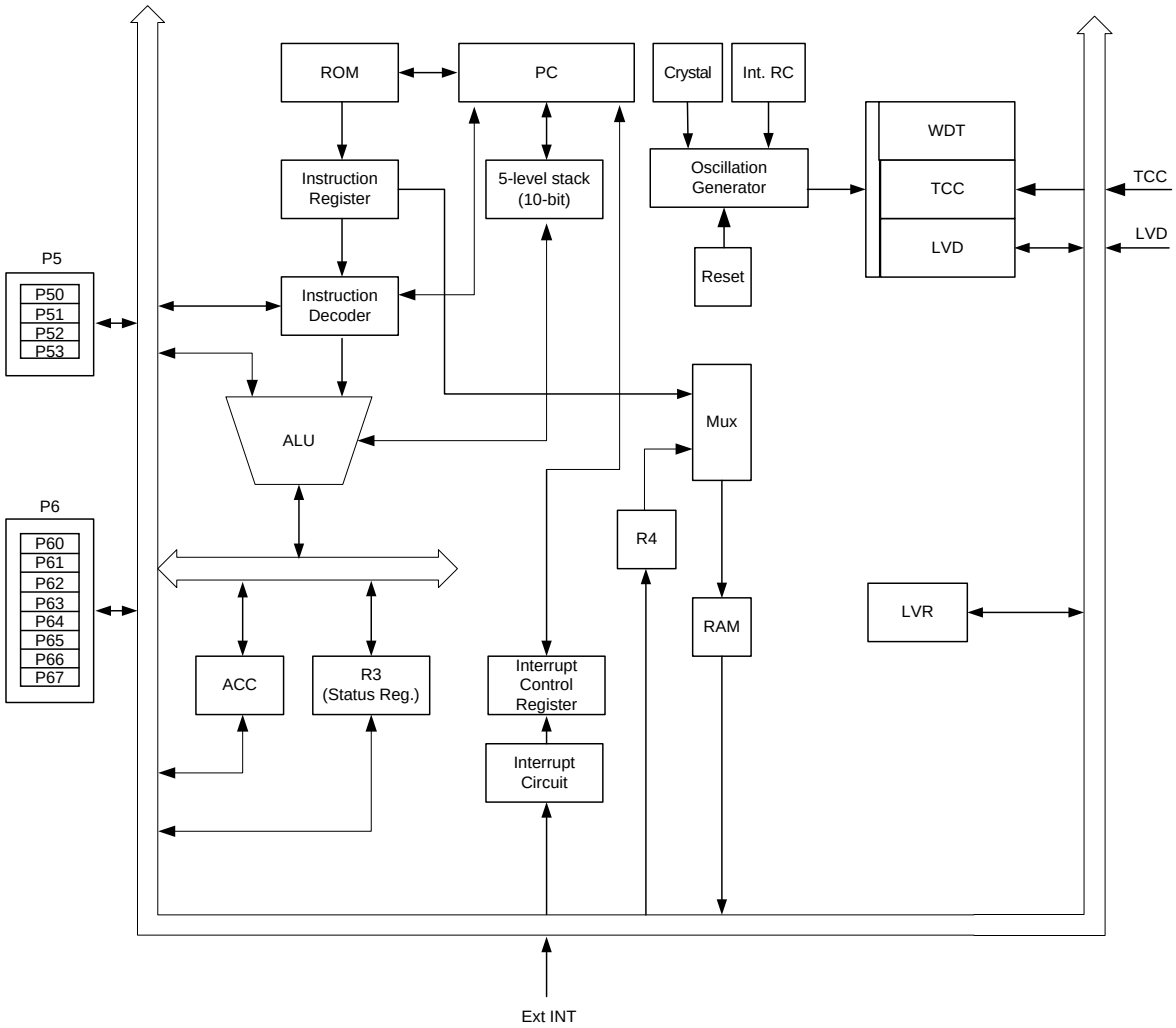


Figure 5-1 EM79F701N Functional Block Diagram

6 Function Description

6.1 Operational Registers

6.1.1 R0: IAR (Indirect Addressing Register)

R0 is not a physically implemented register. It is used as an indirect addressing pointer. Any instruction using R0 as a pointer actually accesses data pointed by the RAM Select Register (R4).

6.1.2 R1: TCCDR (TCC Data Register)

Bit Num	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

• Incremented by an external signal edge, which is defined by TE bit (CONT-4) through the TCC pin, or by the instruction cycle clock.

• Writable and readable as any other registers.

• The prescaler is assigned to TCC, if the PAB bit (CONT-3) is reset.

• When PAB bit is changed at run time, TCCDR will be cleared immediately.

• When PSR2~0 bits ared changed at run time, TCCDR will be cleared immediately.

6.1.3 R2: PCL(Program Counter Low)

Bit Num	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7~0 (PC7~PC0): The low byte of program counter.

• Depending on the device type, R2 and hardware stack are 10-bit wide. The structure is depicted in Figure 6-1.

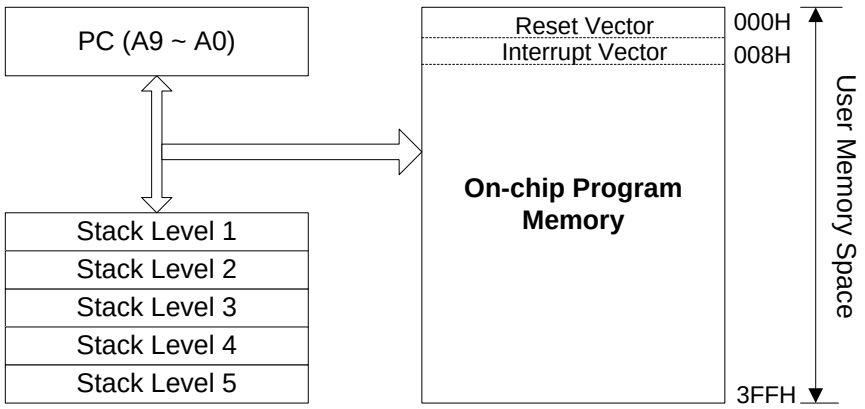


Figure 6-1 Program Counter Organization

• The configuration structure generates 1024×16 bits on-chip program ROM addresses to the relative programming instruction codes. One program page is 1024 words long.

• R2 is set as all "0" when under RESET condition.

• "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows the PC to go to any location within a page.

• "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 are pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.

• "RET" ("RETLk", "RETI") instruction loads the program counter with the contents of the top-level stack.

• "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and tenth bits of the PC will increase progressively.

• "MOV R2, A" allows loading of an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits (A8~A9) of the PC will remain unchanged.

• Any instruction (except “ADD R2,A”) that is written to R2 (e.g., "MOV R2, A", "BC R2, 6" etc.) will cause the ninth bit and above bits to remain unchanged.

• All instructions are single instruction cycle (fclk/2 or fclk/4) except for instructions that would change the contents of R2. Such instructions will need one more instruction cycle.

Address	BANK 0	BANK 1
0X00	IAR (Indirect Addressing Reg.)	
0X01	TCCDR (TCC Data Register)	
0X02	PCL (Program Counter Low)	
0X03	SR (Status Reg.)	
0X04	RSR (RAM Selection Reg.)	
0X05	Port 5	TBHP
0X06	Port 6	TBLP
0X07	Reserved	Reserved
0X08	Reserved	Reserved
0X09	Reserved	Reserved
0X0A	Reserved	Reserved
0x0B	Reserved	Reserved
0X0C	Reserved	Reserved
0X0D	Reserved	Reserved
0X0E	ISR1 / WUCR1	LVDCR / WUCR2
0X0F	ISR2	SYSCON
0X10	General Purpose Register	
.		
.		
0X1F		
0X20	32-Byte Register	
.		
.		
0X3F		
0X40	Reserved	
.		
.		
0XF3		
0XF4	CONT	

Address	BANK 0	BANK 1
0XF5	IOC5 (IOCR5)	
0XF6	IOC6 (IOCR6)	
0XF7	Reserved	
0XF8	Reserved	
0XF9	Reserved	
0XFA	Reserved	
0XFB	IOCB (P56PDCR)	
0XFC	IOCC (P6ODCR)	
0XFD	IOCD (P6PHCR)	
0XFE	IOCE (WDTCR)	
0XFF	IOCF (IMR1)	

Figure 6-2 Data Memory Configuration

6.1.4 R3: SR(Status Register)

Bit Num	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RST	GP1	GP0	T	P	Z	DC	C
Type	F	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (RST): Bit for reset type

0: Set to 0 if the device wakes up from other reset type.

1: Set to 1 if the device wakes up from sleep mode on a pin change, external interrupt or low voltage detector interrupt.

Bits 6 ~ 5 (GP1 ~ GP0): General-purpose read/write bits

Bit 4 (T): Time-out bit

Set to “1” with the "SLEP" and "WDTC" commands, and reset to “0” by WDT time-out.

Bit 3 (P): Power down bit

Set to “1” during power on or by a "WDTC" command; and reset to “0” by a "SLEP" command.

Bit 2 (Z): Zero flag

Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4: RSR(RAM Select Register)

Bit Num	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	GP	BANK	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7: General-purpose read/write bits.

Bit 6 (BANK): Used to select Banks 0~1.

Bits 5~0 (RSR5~RSR0): these bits are used to select registers (address: R0~R3F) in the indirect address mode.

6.1.6 Bank 0 R5: Port 5 (Port 5 I/O Data Register)

Bit Num	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	GP	GP	GP	GP	P53	P52	P51	P50
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 4: General-purpose read/write bits.

Bits 3 ~ 0 (P53 ~ P50): are I/O registers.

6.1.7 Bank 0 R6: Port 6 (Port 6 I/O Data Register)

Bit Num	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	P67	P66	P65	P64	P63	P62	P61	P60
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 ~ 0 (P67 ~ P60): are I/O registers

6.1.8 Bank 0 RE: ISR1/WUCR1 (Interrupt Status 1 and Wake-up Control Register 1)

Bit Num	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	/LVD	LVDIF	-	-	-	-	-	LVDWE
Type	R	F	R	R	R	R	R	R/W

Bit 7 (/LVD): Low voltage Detector state.

When the VDD pin voltage is lower than LVD voltage interrupt level (selected by LVD1 and LVD0), this bit will be cleared.

0: Low voltage is detected

1: Low voltage is not detected or LVD function is disabled

Bit 6 (LVDIF): LVD Interrupt Flag bit.

0: No interrupt occurs

1: With interrupt request

Set when VDD drops slowly and crosses the detect point, reset to “0” by software

Bits 5 ~ 1: Not used. Set to “0” at all time.

Bit 0 (LVDWE): Low Voltage Detect wake-up.

0: Disable Low Voltage Detect wake-up

1: Enable Low Voltage Detect wake-up

6.1.9 Bank 0 RF: ISR2(Interrupt Status Register 2)

Bit Num	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	-	-	-	-	-	EXIF	ICIF	TCIF
Type	R	R	R	R	R	F	F	F

NOTE

" 1 " *means with interrupt request* ***" 0 "*** *means no interrupt occurs*

Bits 7 ~ 3: Not used. Set to "0" at all time.

Bit 2 (EXIF): External Interrupt Flag. Set by a falling edge on the /INT pin, reset by software.

Bit 1 (ICIF): Port 6 input status changed interrupt flag. Set when Port 6 input changes, reset by software.

Bit 0 (TCIF): TCC Overflow Interrupt Flag. Set when TCC overflows, reset by software.

RF can be cleared by instruction but cannot be set.

R4F IOCF is the interrupt mask register.

NOTE

The result of reading RF is the "logic AND" of RF and IOCF.

6.1.10 Bank 1 R5: TBHP (Table Point Register for Instruction TBRD)

Bit Num	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	MLB	-	-	-	-	-	RBit9	RBit8
Type	R/W	R	R	R	R	R	R/W	R/W

Bit 7 (MLB): Chooses the MSB or LSB machine code to move into the register.

The machine code is pointed by TBLP and TBHP register.

MLB	Read to Register data value description
0	Read byte value is Bit7~bit0 from machine code.
1	Read byte value is Highest bit fixed "0" and bit14~bit8 from machine code.

Bits 6 ~ 2: Not used. Set to "0" at all time.

Bits 1 ~ 0: Most 2 significant bits of address for program code

6.1.11 Bank 1 R6: TBLP (Table Point Register for Instruction TBRD)

Bit Num	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RBit7	RBit6	RBit5	RBit4	RBit3	RBit2	RBit1	RBit0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0: These are the least 8 significant bits of address for program code.

NOTE

- *Bank 1 R6 overflow will carry to Bank 1 R5.*
- *Bank 1 R6 underflow will borrow from Bank 1 R5.*

6.1.12 Bank 1 RE: LVDCR/WUCR2 (LVD Control and Wake-up Register 2)

Bit Num	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LVDIE	LVDEN	LVD1	LVD0	-	-	-	EXWE
Type	R/W	R/W	R/W	R/W	R	R	R	R/W

NOTE

- *The Bank 1-RE <7> register is both readable and writable.*
- Individual interrupt is enabled by setting its associated control bit in the *Bank 1-RE<7> to "1."*
- *Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 6-10(Interrupt Input Circuit) in Section 6.6 (Interrupt)*
- *After LVDEN bit is set, you must wait at least 40us to stabilize LVD. If you go to sleep immediately after setting LVDEN, LVD will not work normally.*

Bit 7 (LVDIE): Low voltage detector interrupt enable bit

0: Disable the low voltage detector interrupt

1: Enable the low voltage detector interrupt

Bit 6 (LVDEN): Low voltage detector enable bit

0: Disable the Low voltage detector function

1: Enable the Low voltage detector function

Bits 5 ~ 4(LVD1~0): Low voltage detector level bits

LVDEN	LVD1, LVD0	LVD Voltage Interrupt Level	/LVD
1	11	Vdd ≤ 2.2V	0
		Vdd > 2.2V	1
1	10	Vdd ≤ 3.3V	0
		Vdd > 3.3V	1
1	01	Vdd ≤ 4.0V	0
		Vdd > 4.0V	1
1	00	Vdd ≤ 4.5V	0

LVDEN	LVD1, LVD0	LVD Voltage Interrupt Level	/LVD
		Vdd > 4.5V	1
0	××	N/A	1

NOTE

IF Vdd has crossover at LVD voltage in interrupt level as VDD varies, LVD interrupt will occur.

Bits 3 ~ 1: Not used. Set to “0” at all time.

Bit 0 (EXWE): External /INT wake-up enable bit

0: Disable External /INT pin wake-up

1: Enable External /INT pin wake-up

6.1.13 Bank 1 RF: SYSCON (System Control Register)

Bit Num	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	-	TIMERSC	CPUS	IDLE	-	-	RCM1	RCM0
Type	-	R/W	R/W	R/W	-	-	R/W	R/W

Bits 7, 3 ~ 2: Not used. Set to "0" all the time.

Bit 6 (TIMERSC): TCC clock source select.

0: F_S

1: F_M / 2 or F_M / 4 (Default)

Bit 5 (CPUS): CPU Oscillator Source Select

0: Fs: sub frequency for WDT internal RC time base 16 kHz

1: Fm: main oscillator (F_M) (Default)

When CPUS = 0, the CPU oscillator selects the sub-oscillator and the main oscillator is stopped.

Bit 4 (IDLE): Idle Mode Enable Bit.

From SLEP instruction, this bit will determine as to which mode to choose.

0: IDLE = ‘0’ + SLEP instruction → sleep mode (Default)

1: IDLE = ‘1’ + SLEP instruction → idle mode

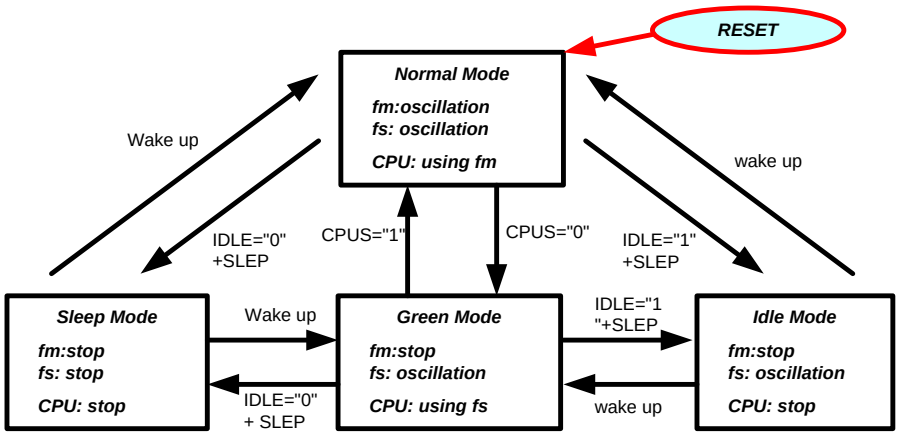


Figure 6-3 CPU Operation Mode Diagram

The MCU reset and warm up time reference below table:

Fm	Fs	Power-on/LVR	Pin-Reset / WDT	
			N / G	S / I
HIRC	LIRC	(256/64/16/4)ms + WSTO + 8/Fm[1]	WSTO + 8*1/Fm + 2/F128K	WSTO + 8*1/Fm + 2/F128K
HXT1/HXT2/XT/LXT1	LIRC	(256/64/16/4)ms + WSTO +510/Fm[1]	WSTO + 510*1/Fm + 2/F128K	WSTO + 510*1/Fm + 2/F128K
LXT2	LIRC	(256/64/16/4)ms + WSTO +254/Fm[1]	WSTO + 254*1/Fm + 2/F128K	WSTO + 254*1/Fm + 2/F128K

The CPU Operation Mode change time reference below table:

Fm	Fs	G → N	I → N	S → N
HIRC	LIRC	WSTO + 1.5/Fs + 6/Fm	WSTO + 8*1/Fm	WSTO + 8*1/Fm
LXT1 / HXT1 / HXT2 / XT	LIRC	WSTO + 1.5/Fs + 510/Fm	WSTO + 510*1/Fm	WSTO + 510*1/Fm
LXT2	LIRC	WSTO + 1.5/Fs + 254*1/Fm	WSTO + 254*1/Fm	WSTO + 254*1/Fm

Fm	Fs	I → G	S → G
HIRC	LIRC	8*1/Fs	WSTO + 8*1/Fs
LXT1 / HXT1 / HXT2 / XT/LXT2	LIRC	8*1/Fs	WSTO + 8*1/Fs

WSTO: Waiting Time from Start-to-Oscillation

N: Normal mode G: Green mode I: Idle mode S: Sleep mode

Notes:

[1]*The warm up time define base on the code option WDTPS1~0 bits. (Refer to Table 8)*

Bits 3 ~ 2: Not used. Set to "0" all the time.

Bits 1 ~ 0 (RCM1 ~ RCM0): IRC mode select bits.

RCM 1	RCM 0	Frequency (MHz)
1	1	4
1	0	16
0	1	8
0	0	1

NOTE

- *The initial values of Bank1 RF<1, 0> will be kept the same as Word 1<6, 5>.*
- *If user changes the IRC frequency from A-frequency to B-frequency, the MCU needs to wait for some time for it to work. The waiting time corresponds to the B-frequency.*

6.1.14 R10 ~ R3F

These are all 8-bit general-purpose registers.

6.2 Special Purpose Registers

6.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator, which is not an addressable register.

6.2.2 CONT (Control Register)

Bit Num	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	GP	INT	TS	TE	PAB	PSR2	PSR1	PSR0
Type	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (GP): General purpose register.

Bit 6 (INT): Interrupt enable flag

0: masked by DISI or hardware interrupt

1: enabled by ENI/RETI instructions

This bit is readable only.

Bit 5 (TS): TCC signal source

0: internal instruction cycle clock, P62 is a bidirectional I/O pin.

1: transition on TCC pin

NOTE

■*The priority of TS is higher than IOC62.*

■ *When TS is set, P62 pin change/interrupt and pull-high are disabled.*

Bit 4 (TE): TCC Signal Edge

0: increment if the transition from low to high takes place on TCC pin

1: increment if the transition from high to low takes place on TCC pin

Bit 3 (PAB): Prescaler Assigned Bit

0: TCC

1: WDT

Bit 2 ~ Bit 0 (PSR2 ~ PSR0): TCC/WDT prescaler bits

PSR2	PSR1	PSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

The CONT register is both readable and writable.

6.2.3 IOC5 (I/O Port 5 Control Register)

Bit Num	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	-	-	-	-	IOC53	IOC52	IOC51	IOC50
Type	R	R	R	R	R/W	R/W	R/W	R/W

Bits 7 ~ 4: Not used. Set to “0” all the time.

Bits 3 ~ 0 (IOC53 ~ IOC50):

0: defines the relative I/O pin as output

1: puts the relative I/O pin into high impedance

6.2.4 IOC6 (I/O Port 6 Control Register)

Bit Num	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7 ~ 0 (IOC67 ~ IOC60):

0: defines the relative I/O pin as output

1: puts the relative I/O pin into high impedance

6.2.5 IOCB (P56PDCR: Port 5 and Port 6 Pull-down Contorl Register)

Bit Num	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	/PD63	/PD62	/PD61	/PD60	GP	/PD52	/PD51	/PD50
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (/PD63): Control bit used to enable pull-down of the P63 pin.

0: Enable internal pull-down

1: Disable internal pull-down

Bit 6 (/PD62): Control bit used to enable pull-down of the P62 pin.

Bit 5 (/PD61): Control bit used to enable pull-down of the P61 pin.

Bit 4 (/PD60): Control bit used to enable pull-down of the P60 pin.

Bit 3: General-purpose read/write bit.

Bit 2 (/PD52): Control bit used to enable pull-down of the P52 pin.

Bit 1 (/PD51): Control bit used to enable pull-down of the P51 pin.

Bit 0 (/PD50): Control bit used to enable pull-down of the P50 pin.

The IOCB Register is both readable and writable.

6.2.6 IOCC (P6ODCR: Port 6 Open-drain Control Register)

Bit Num	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OD67	OD66	OD65	OD64	GP	OD62	OD61	OD60
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (OD67): Control bit used to enable open-drain of the P67 pin.

0: Disable open-drain output

1: Enable open-drain output

Bit 6 (OD66): Control bit used to enable open-drain of the P66 pin.

Bit 5 (OD65): Control bit used to enable open-drain of the P65 pin.

Bit 4 (OD64): Control bit used to enable open-drain of the P64 pin.

Bit 3: General-purpose read/write bit.

Bit 2 (OD62): Control bit used to enable open-drain of the P62 pin.

Bit 1 (OD61): Control bit used to enable open-drain of the P61 pin.

Bit 0 (OD60): Control bit used to enable open-drain of the P60 pin. (If EIS=1, P60 open-drain is disabled.)

The IOCC Register is both readable and writable.

6.2.7 IOCD (P6PHCR: Port 6 Pull-high Control Register)

Bit Num	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	/PH67	/PH66	/PH65	/PH64	GP	/PH62	/PH61	/PH60
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (/PH67): Control bit is used to enable pull-high of the P67 pin.

0: Enable internal pull-high

1: Disable internal pull-high

Bit 6 (/PH66): Control bit used to enable pull-high of the P66 pin.

Bit 5 (/PH65): Control bit used to enable pull-high of the P65 pin.

Bit 4 (/PH64): Control bit used to enable pull-high of the P64 pin.

Bit 3: General-purpose read/write bit.

Bit 2 (/PH62): Control bit used to enable pull-high of the P62 pin.

Bit 1 (/PH61): Control bit used to enable pull-high of the P61 pin.

Bit 0 (/PH60): Control bit used to enable pull-high of the P60 pin.

The IOCD Register is both readable and writable.

6.2.8 IOCE (WDTCR: WDT Control Register)

Bit Num	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	WDTE	EIS	GP	GP	GP	GP	GP	GP
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 7 (WDTE): Control bit used to enable the Watchdog timer.

0: Disable WDT

1: Enable WDT

Bit 6 (EIS): Control bit is used to define the function of P60 (/INT) pin.

0: P60, bidirectional I/O pin. (default)

1: /INT, external interrupt pin.

When EIS is "0," the path of /INT is masked.

When EIS is "1", the status of /INT pin can also be read by way of reading Port 6 (R6). See Figure 6-7 under Section 6.4 for reference.

When EIS is "1", P60 pin change/interrupt and pull-high are disabled.

Bits 5 ~ 0: General purpose register.

6.2.9 IOCF (IMR1: Interrupt Mask Register)

Bit Num	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	-	-	-	-	-	EXIE	ICIE	TCIE
Type	R	R	R	R	R	R/W	R/W	R/W

Bits 7 ~ 3: Not used. Set to “1” at all time.

Bit 2 (EXIE): EXIF interrupt enable bit

0: disable EXIF interrupt

1: enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit

0: disable ICIF interrupt

1: enable ICIF interrupt

Bit 0 (TCIE): TCIF interrupt enable bit

0: disable TCIF interrupt

1: enable TCIF interrupt

Individual interrupt is enabled by setting its associated control bit in the IOCF to "1". Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 6-10.

The IOCF register is both readable and writable.

6.3 TCC/WDT and Prescaler

There is an 8-bit counter available as prescaler for the TCC or WDT. The prescaler is available for the TCC only or the WDT only and the PAB bit of the CONT register is used to determine the prescaler assignment. The PSR0~PSR2 bits determine the ratio. The prescaler is cleared each time the instruction is written to TCC under TCC mode. The WDT and prescaler, when assigned to WDT mode, are cleared by the "WDTC" or "SLEP" instructions. Figure 6-4 depicts the circuit diagram of TCC. Figure 6-5 depicts the circuit diagram of WDT.

- R1 (TCC) is an 8-bit timer/counter. The TCC clock source can be internal or external clock input (edge selectable from TCC pin). If the TCC signal source is from an internal clock, TCC will be incremented by 1 every instruction cycle (without prescaler). Referring to Figure 6-4, CLKS= F_M / 2 or CLKS= F_M / 4, depends on the Code Option bit CLKS. CLKS= F_M / 2 is used if CLKS bit is "0", and CLKS= F_M / 4 is used if CLKS bit is "1". If the TCC signal source is from an external clock input, TCC is incremented by 1 at every falling edge or rising edge of the TCC pin.

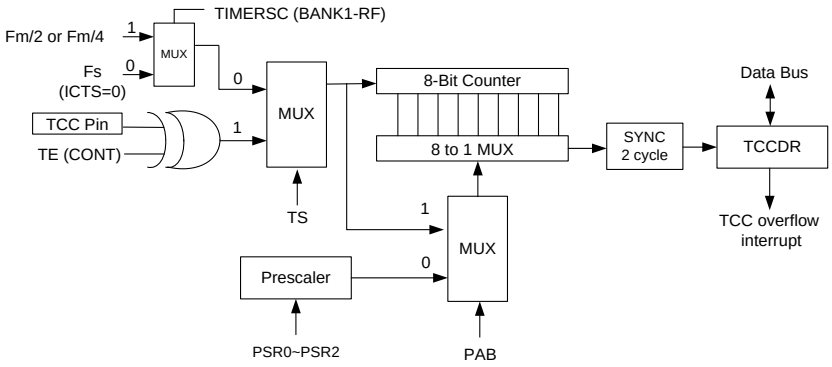


Figure 6-4 TCC Block Diagram

- The Watchdog Timer is a free running on-chip RC oscillator. The WDT will keep running even when the oscillator driver has been turned off (i.e. in sleep mode) if WDT is enabled (ENWDT=0 & WDTE=1). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled any time during normal mode by software programming. Refer to WDTE bit of the IOCE register. Without prescaler, the WDT time-out period is approximately 18 ms (Default).

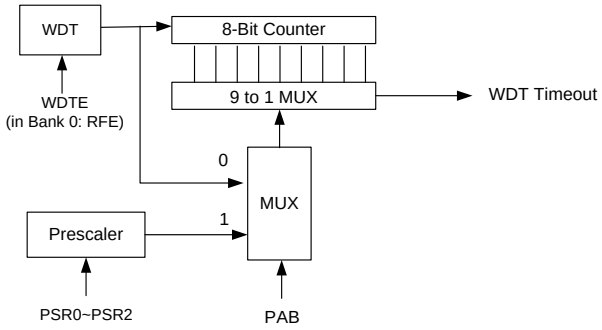
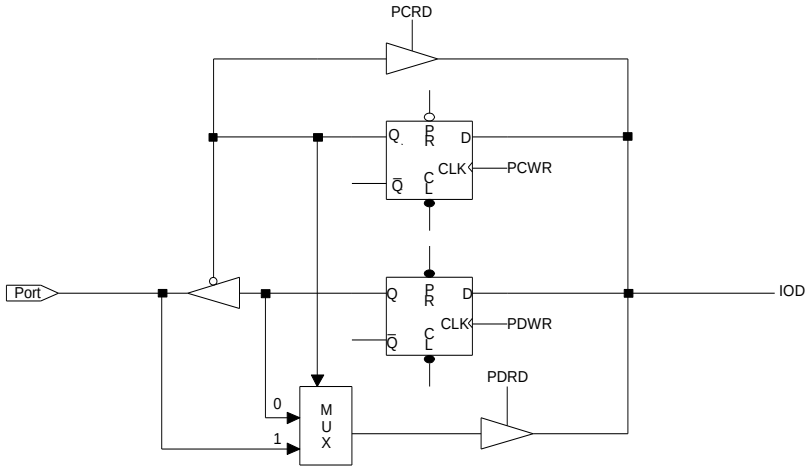


Figure 6-5 WDT Block Diagram

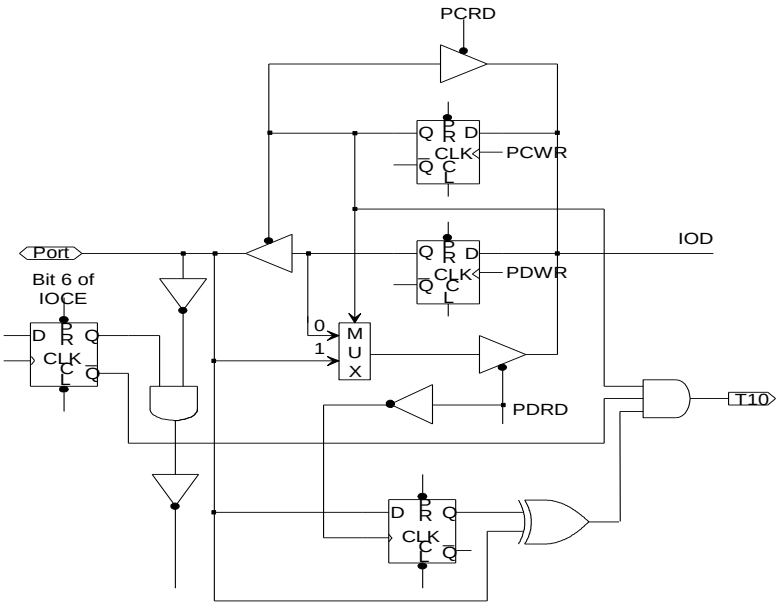
6.4 I/O Ports

The I/O registers, both Port 5 and Port 6 are bidirectional tri-state I/O ports. Port 6 can be pulled-high internally by software except P63. In addition, Port 6 can also have open-drain output by software except P63. Input status changed interrupt (or wake-up) function is available from Port 6. P50 ~ P52, and P60 ~ P63 pins can be pulled-down by software. Each I/O pin can be defined as "input" or "output" pin by the I/O control register (IOC5 ~ IOC6). The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5 and Port 6 are shown in Figures 6-6 ~ Figure 6-8 respectively.



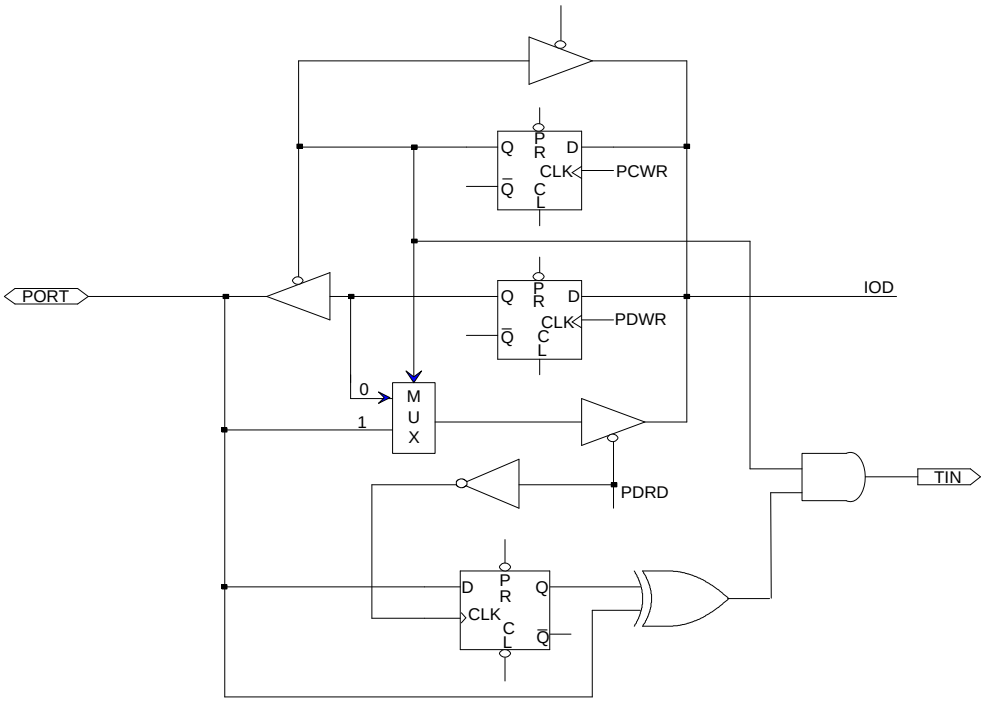
Note: Pull-down is not shown in the figure.

Figure 6-6 I/O Port and I/O Control Register Circuit for Port 5 and 6



Note: Pull-high (down) and open-drain are not shown in the figure.

Figure 6-7 I/O Port and I/O Control Register Circuit for P60 (/INT)



Note: Pull-high (down) and open-drain are not shown in the figure.

Figure 6-8 I/O Port and I/O Control Register Circuit for P61~P67

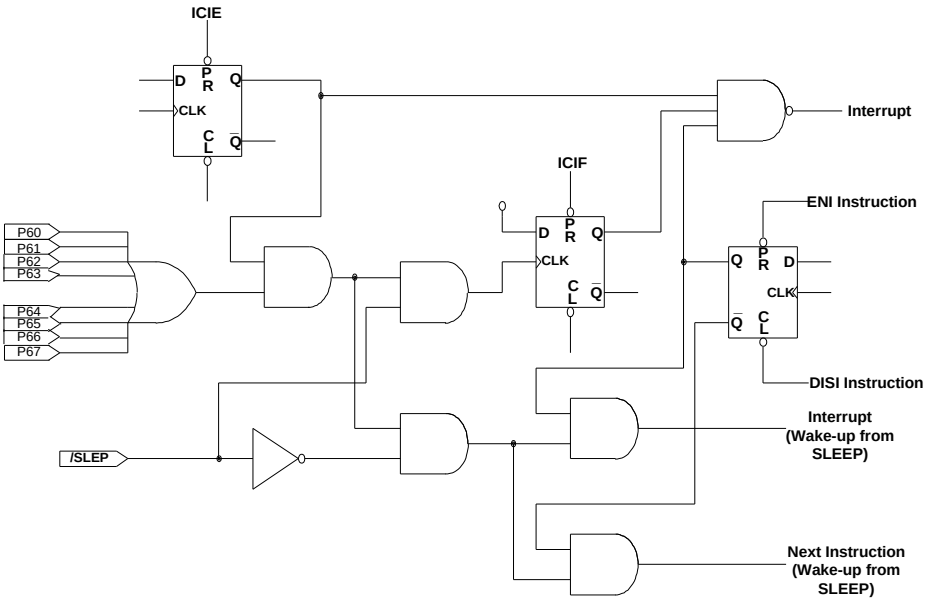


Fig. 6-9 Block Diagram of I/O Port 6 with input change interrupt/wake-up

Table 1 Usage of Port 6 Input Change Wake-up/Interrupt Function

Usage of Port 6 Input Status Change Wake-up/Interrupt	
(I) Wake-up from Port 6 Input Status Change (a) Before Sleep 1. Disable WDT 2. Read I/O Port 6 (MOV R6,R6) 3. Execute "ENI" or "DISI" 4. Enable interrupt (Set IOCF.1) 5. Execute "SLEP" instruction (b) After Wake-up 1. IF "ENI" → Interrupt vector (008H) 2. IF "DISI" → Next instruction	(II) Port 6 Input Status Change Interrupt 1. Read I/O Port 6 (MOV R6,R6) 2. Execute "ENI" 3. Enable interrupt (Set IOCF.1) 4. IF Port 6 change (interrupt) → Interrupt vector (008H)

NOTE

Port 5 and Port 6 I/O state will be initialized as 1 after a reset. Hence, assign I/O state before configure I/O as output is suggested to prevent unexpected output state appearing after a reset occurs.

Example:

```
MOV A, @0X00
MOV PORT6,A    ; assign I/O state in advance
MOV A, @0X00
MOV IOCR6,A    ; configure I/O as output
```

6.5 Reset and Wake-up

6.5.1 Reset

A Reset is initiated by one of the following events:

1) Power-on reset

2) /RESET pin input "low"

3) WDT time-out (if enabled)

4) Low Voltage Reset

The device is kept under reset condition for a period of approximately 18ms (one oscillator start-up timer period) or 150 µs (Events 1 and 4 are approximately 18 ms and Events 2 and 3 are approximately 150 µs) after a reset is detected. Once a Reset occurs, the following functions are performed**:**

- The oscillator is running, or will be started.
- The Program Counter (R2) is set to all "0."
- All I/O port pins are configured as input mode (high-impedance state)
- The Watchdog timer and prescaler are cleared.
- When power is switched on, the upper 3 bits of R3 are cleared.
- The bits of the CONT register are set to all "1" except for Bit 6 (INT flag).
- The bits of the IOCB register are set to all "1."
- The IOCC register is cleared.
- The bits of the IOCD register are set to all "1."
- Bit 7 of the IOCE register is set to "1," and Bit 6 is cleared.
- Bits 0 ~ 2 of Bank 0 RF and Bits 0 ~ 2 of IOCF registers are cleared.
- The bits of the control register are set as Table shown in Section 6.5.4.

Sleep (power down) mode is asserted by executing the “SLEP” instruction. While entering Sleep mode, WDT (if enabled) is cleared but keeps on running. After a wake-up in IRC mode (IRC 4 MHz / 5V), wake-up time is 1.5 µs, XT mode (4 MHz / 5V) wake-up time is 1.5 ms.

The controller can be awakened by:

1) External reset input on /RESET pin,

2) WDT time-out (if enabled)

3) Port 6 input status changes (if ICIE enabled) (If EIS=1, P60 pin change interrupt/wake-up is disabled.)

4) External (P60, /INT) pin changes (if EXWE is enabled)

5) Low voltage detector (if LVDWE is enabled).

The first two cases will cause the EM79F701N to reset. The T and P flags of R3 are used to determine the source of the reset (wake-up). The last case is considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being

executed) determines whether or not the controller branches to the interrupt vector following a wake-up. If ENI is executed before SLEP, the instruction will begin to execute from Address 008H after a wake-up. If DISI is executed before SLEP, the operation will restart from the succeeding instruction right next to SLEP after a wake-up.

After a wake-up in IRC mode (IRC 4 MHz / 5V), the wake-up time is 1.5 μs, in XT mode (4 MHz / 5V), the wake-up time is 1.5 ms.

One or more of Cases 2 and 5 can be enabled before going into Sleep mode. That is,

[a] if WDT is enabled before SLEP, Port 6 Input Status Change Interrupt must be disabled. Hence, the EM79F701N can be awakened only by Case 1 or Case 2. Refer to Section 6.6, Interrupt for further details.

[b] if Port 6 Input Status Change Interrupt is enabled before SLEP, WDT must be disabled. Hence, the EM79F701N can be awakened only by Case 1 or Case 3.

[c] if External (P60,/INT) pin change is used to wake-up EM79F701N and EXWE bit of Bank 1-RE register is enabled before SLEP, WDT must be disabled. Hence, the EM79F701N can be waken-up only by Case 1 or Case 4.

[d] if Low voltage detector is used to wake up the EM79F701N and LVDWE bit of Bank 0-RE register is enabled before SLEP, the WDT must be disabled by software. Hence, the EM79F701N can be awakened only by Case 1 or Case 5.

If Port 6 Input Status Change Interrupt is used to wake-up the EM79F701N (Case [b] above), the following instructions must be executed before SLEP:

```
MOV A, @xxxx1110b     ; Select the WDT prescaler, it must be
                      ; set over 1:1
MOV CONT, A
WDTC                  ; Clear WDT and prescaler
MOV A, @0xxxxxxxb     ; Disable WDT
MOV WDTCR, A
MOV R6, R6            ; Read Port 6
MOV A, @00000x1xb     ; Enable Port 6 input change interrupt
MOV IMR1, A
ENI (or DISI)         ; Enable (or disable) global interrupt
SLEP                  ; Sleep
```

NOTE

1. After waking up from sleep mode, WDT is automatically enabled. The WDT enable/disable operation after waking up from sleep mode should be appropriately defined in the software.

2. To avoid a reset from occurring when the Port 6 Input Status Changed Interrupt enters into an interrupt vector or is used to wake-up the MCU, the WDT prescaler must be set above 1:1 ratio.

6.5.2 Wake-up and Interrupt Modes Operation Summary

The controller can be awakened from sleep mode and idle mode. The wake-up signals are listed as follows.

Wake-up Signal	Condition Signal	Sleep Mode		Idle Mode		Green Mode		Normal Mode	
		DISI	ENI	DISI	ENI	DISI	ENI	DISI	ENI
External INT	EXWE = 0 EXIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	EXWE = 0 EXIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	EXWE = 1 EXIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	EXWE = 1 EXIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Port 6 Pin change	ICIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	ICIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
TCC Overflow	TCIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	TCIE = 1			Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
Low Voltage Detector	LVDWE = 0 LVDIE = 0	Wake-up is invalid		Wake-up is invalid		Interrupt is invalid		Interrupt is invalid	
	LVDWE = 0 LVDIE = 1	Wake-up is invalid		Wake-up is invalid		Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector
	LVDWE = 1 LVDIE = 0	Wake up + Next Instruction		Wake up + Next Instruction		Interrupt is invalid		Interrupt is invalid	
	LVDWE = 1 LVDIE = 1	Wake up + Next Instruction	Wake up + Interrupt Vector	Wake up + Next Instruction	Wake up + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector	Next Instruction	Interrupt + Interrupt Vector

6.5.3 Summary of Registers Initialized Values

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×00	R0 (IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×01	R1 (TCCDR)	Bit Name	TCC7	TCC6	TCC5	TCC4	TCC3	TCC2	TCC1	TCC0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×02	R2 (PCL)	Bit Name	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	Jump to Address 0x08 or continue to execute next instruction							
0x03	R3 (SR)	Bit Name	RST	GP1	GP0	T	P	Z	DC	C
		Power-on	0	0	0	U	1	U	U	U
		/RESET and WDT	0	0	0	*	*	P	P	P
		Wake-up from Pin Change	P	P	P	*	*	P	P	P
0x04	R4 (RSR)	Bit Name	GP	BANK	RSR5	RSR4	RSR3	RSR2	RSR1	RSR0
		Power-on	0	0	1	1	1	1	1	1
		/RESET and WDT	0	0	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0x05	BANK 0, R5 (PORT 5)	Bit Name	GP	GP	GP	GP	P53	P52	P51	P50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×06	BANK 0, R6 (PORT 6)	Bit Name	P67	P66	65	P64	P63	P62	P61	P60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	BANK 0, RE (ISR1/WUCR1)	Bit Name	/LVD	LVDIF	×	×	×	×	×	LVDWE
		Power-on	1	0	0	0	0	0	0	0
		/RESET and WDT	1	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	0	0	0	0	0	P
0×0F	BANK 0, RF (ISR2)	Bit Name	×	×	×	×	×	EXIF	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	0	0	0	0	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×05	BANK 1, R5 (TBHP)	Bit Name	MLB	×	×	×	×	×	RBit 9	RBit 8
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	0	0	0	0	0	P	P
0×06	BANK 1, R6 (TBLP)	Bit Name	RBit7	RBit 6	RBit 5	RBit 4	RBit 3	RBit 2	RBit 1	RBit 0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×0E	BANK 1, RE (LVDCR/WUCR2)	Bit Name	LVDIE	LVDEN	LVD1	LVD0	×	×	×	EXWE
		Power-on	0	0	1	1	0	0	0	0
		/RESET and WDT	0	0	1	1	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	0	0	0	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0×0F	BANK 1, RF (SYSCON)	Bit Name	×	TIMERSC	CPUS	IDLE	×	×	RCM1	RCM0
		Power-on	0	1	1	0	0	0	WORD1 <6,5>	
		/RESET and WDT	0	1	1	0	0	0		
		Wake-up from Pin Change	P	P	P	P	0	0	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xF4	CONT	Bit Name	GP	INT	TS	TE	PAB	PSR2	PSR1	PSR0
		Power-on	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0xF5	IOC5 (IOCR5)	Bit Name	×	×	×	×	IOC53	IOC52	IOC51	IOC50
		Power-on	0	0	0	0	1	1	1	1
		/RESET and WDT	0	0	0	0	1	1	1	1
		Wake-up from Pin Change	0	0	0	0	P	P	P	P
0xF6	IOC6 (IOCR6)	Bit Name	IOC67	IOC66	IOC65	IOC64	IOC63	IOC62	IOC61	IOC60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×FB	IOCB (P56PDCR)	Bit Name	/PD63	/PD62	/PD61	/PD60	GP	/PD52	/PD51	/PD50
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×FC	IOCC (P6ODCR)	Bit Name	OD67	OD66	OD65	OD64	GP	OD62	OD61	OD60
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×FD	IOCD (P6PHCR)	Bit Name	/PH67	/PH66	/PH65	/PH64	GP	/PH62	/PH61	/PH60
		Power-on	1	1	1	1	1	1	1	1
		/RESET and WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×FE	IOCE (WDTCR)	Bit Name	WDTE	EIS	GP	GP	GP	GP	GP	GP
		Power-on	1	0	1	1	1	1	1	1
		/RESET and WDT	1	0	1	1	1	1	1	1
		Wake-up from Pin Change	P	P	P	P	P	P	P	P
0×FF	IOCF (IMR1)	Bit Name	×	×	×	×	×	EXIE	ICIE	TCIE
		Power-on	1	1	1	1	1	0	0	0
		/RESET and WDT	1	1	1	1	1	0	0	0
		Wake-up from Pin Change	1	1	1	1	1	P	P	P

Legend: **×:** Not used **U:** Unknown or don't care **P:** Previous value before reset

* Refer to the tables provided in the next section (Section 6.5.4).

6.5.4 Status of RST, T, and P of the Status Register

A Reset condition is initiated by the following events

1) A power-on condition
2) A high-low-high pulse on /RESET pin
3) Watchdog timer time-out
4) Low Voltage Reset

The values of RST, T and P listed in the table below are used to check how the processor wakes up.

Table 2 Values of RST, T, and P after a Reset

Reset Type	RST	T	P
Power on	0	U	1
/RESET during Operation mode	0	*P	*P
/RESET wake-up during Sleep mode	0	1	0
/RESET wake-up during Idle mode	0	1	0
WDT time-out during Operation mode	0	0	*P
WDT wake-up during Sleep mode	0	0	0
WDT wake-up during Idle mode	0	0	0
Wake-up on pin change during Sleep mode	1	1	0
Wake-up on pin change during Idle mode	P	1	0
Wake-up on external interrupt during Sleep mode	1	1	0
Wake-up on external interrupt during Idle mode	P	1	0
Wake-up on LVD interrupt during Sleep mode	1	1	0
Wake-up on LVD interrupt during Idle mode	P	1	0
Low Voltage Reset	0	*P	*P

* ***P:*** *Previous status before reset,* ***U:*** *Unknown or don't care*

The following table shows the events that may affect the status of T and P.

Table 3 Status of T and P Being Affected by Events

Event	RST	T	P
WDTC instruction	*P	1	1
SLEP instruction	*P	1	0

NOTE

After a power-on reset, the Time-out bit T is unknown. To implement different initialization procedures, it is recommended to check the value of P flag at the beginning of the program. If P flag is set to 1, it indicates power-on reset condition; if P flag is set to 0, proceed to check the value of T flag.

Example:

```
Start:
  JBS SR,P          ;P=1: power-on condition.
  JMP WDT_detect    ;P=0: continue to check WDT status.
POR_Init:
```

```
    (…)              ;POR Initial program
    JMP Main
  WDT_detect:
    JBC   SR,T       ;T=0: WDT time-out condition.
    JMP Main
  WDT_Init:
    (…)
    JMP   Main
```

6.6 Interrupt

The EM79F701N has five interrupts as listed below**:**

Interrupt Source		Enable Condition	Int. Flag	Int. Vector
Internal / External	Reset	-	-	0
External	/INT pin	EXIE	EXIF, CONT-INT	8
External	Port 6 Pin Change	ICIE	ICIF, CONT-INT	8
Internal	TCC	TCIE	TCIF, CONT-INT	8
Internal	LVD	LVDIE	LVDIF, CONT-INT	8

Before the Port 6 Input Status Changed Interrupt is enabled, reading Port 6 (e.g. "MOV R6,R6") is necessary. Each pin of Port 6 will have this feature if its status changes. Any pin configured as output or P60 pin configured as /INT, is excluded from this function. The Port 6 Input Status Changed Interrupt can wake up the EM79F701N from Sleep mode if Port 6 is enabled prior to going into Sleep mode by executing SLEP instruction. When the chip wakes-up, the controller will continue to execute the program in-line if the global interrupt is disabled. If the global interrupt is enabled, it will branch to the interrupt Vector 008H.

RF is the interrupt status register that records the interrupt requests in the relative flags/bits. IOCF is an interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (enabled) occurs, the next instruction will be fetched from Address 008H. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (RF) is set regardless of the status of its mask bit or the execution of ENI. Note that the outcome of RF will be the logic AND of RF and IOCF (refer to Fig. 6-10). The RETI instruction ends the interrupt routine and enables the global interrupt (the execution of ENI).

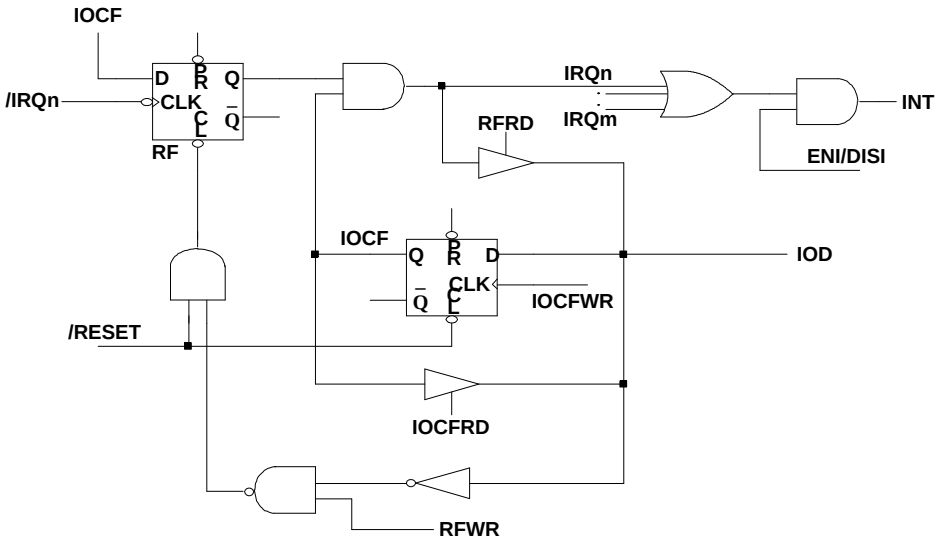


Figure 6-10 Interrupt Input Circuit

Before an interrupt subroutine is executed, the contents of ACC and the R3[6:5], R3[2:0] and R4 registers will be saved by the hardware. If another interrupt occurs, the ACC, R3[6:5], R3[2:0], and R4 will be replaced by the new interrupt. After the interrupt service routine is completed, the ACC, R3[6:5], R3[2:0], and R4 registers are restored.

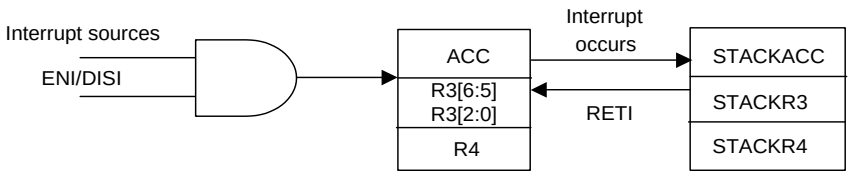


Figure 6-11 Interrupt Backup Diagram

6.7 Oscillator

6.7.1 Oscillator Modes

The EM79F701N can be operated in three different oscillator modes, such as Internal RC oscillator mode (IRC), High Crystal oscillator mode (XT, HXT1/2) and Low Crystal Oscillator mode (LXT1/2). The desired mode can be selected by programming OSC3~0 in the Code Option register. The Table below describes how these three oscillator modes are defined.

Table 4 Oscillator Modes Defined by OSC

Oscillator Modes	OSC3	OSC2	OSC1	OSC0
IRC[1] (Internal RC oscillator mode); P64/RCOUT act as P64	0	0	0	X
IRC[1] (Internal RC oscillator mode); P64/RCOUT act as P64	0	0	1	0
IRC[1] (Internal RC oscillator mode); P64/RCOUT act as RCOUT	0	0	1	1
LXT1[2] (Frequency range of LXT1 mode is 100kHz ~1MHz)	0	1	0	0
HXT1[2] (Frequency range of HXT1 mode is 12 MHz~20 MHz)	0	1	0	1
LXT2[2] (Frequency range of LXT2 mode is 32.768kHz)	0	1	1	0
HXT2[2] (Frequency range of HXT2 mode is 6 MHz~12 MHz)	0	1	1	1
IRC[1] (Internal RC oscillator mode); P64/RCOUT act as P64	1	0	X	X
IRC[1] (Internal RC oscillator mode); P64/RCOUT act as P64	1	1	0	0
IRC[1] (Internal RC oscillator mode); P64/RCOUT act as P64	1	1	0	1
IRC[1] (Internal RC oscillator mode); P64/RCOUT act as P64	1	1	1	0
XT[2] (Frequency range of XT mode is 6 MHz~1 MHz) (default)	1	1	1	1

[1] In IRC mode, crystal mode is disabled, and oscillator pins, OSCO and OSCI, are set as normal I/O pins .

[2] In LXT1, LXT2, HXT1, HXT2 and XT modes; OSCI and OSCO are used as oscillator pins. These pins cannot and should not be defined as normal I/O pins

The maximum operational frequency of the crystal/resonator under different VDDs is as listed below.

Table 5 Summary of Maximum Operating Speeds

Conditions	VDD	Max Freq. (MHz)
One instruction cycle with two clocks	2.1	4.0
	3.0	8.0
	5.0	20.0

6.7.2 Crystal Oscillator/Ceramic Resonators (Crystal)

The EM79F701N can be driven by an external clock signal through the OSCI pin as shown in the following figure.

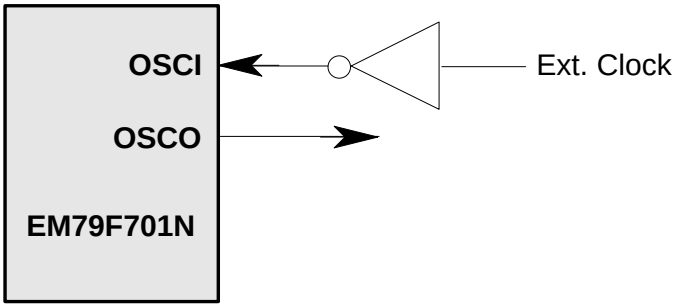


Fig. 6-12 Circuit for External Clock Input

In most applications, pin OSCI and pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. This circuit is depicted in Fig. 6-13. It is the same in both HXT AND LXT modes.

In Fig. 6-14, when the connected resonator in OSCI and OSCO is used in applications, 1 MΩ R1 needs to be shunted with resonator.

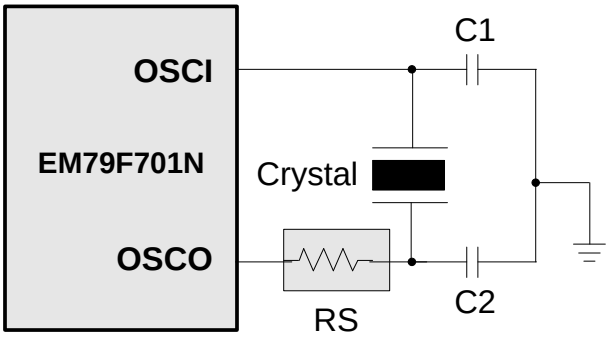


Fig. 6-13 Circuit for Crystal/Resonator

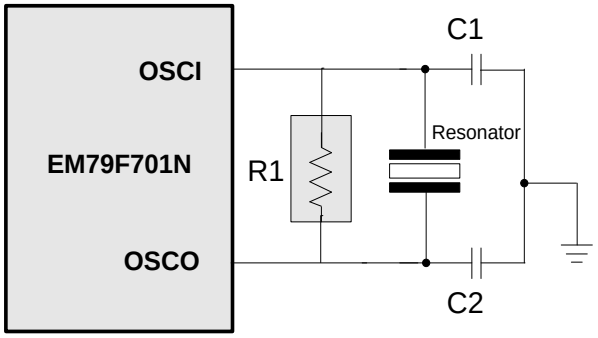


Fig. 6-14 Circuit for Crystal/Resonator

The following table provides the recommended values of C1 and C2. Since each resonator has its own attribute, refer to its specification for appropriate values of C1 and C2. A serial resistor RS may be necessary for AT strip cut crystal or low frequency mode.

Table 6 Capacitor Selection Guide for Crystal Oscillator or Ceramic Resonator

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	LXT1 (100K~1 MHz)	100kHz	60pF	60pF
		200kHz	60pF	60pF
		455kHz	40pF	40pF
		1 MHz	30pF	30pF
	XT (1M~6 MHz)	1.0 MHz	30pF	30pF
		2.0 MHz	30pF	30pF
		4.0 MHz	20pF	20pF
Crystal Oscillator	LXT2 (32.768kHz)	32.768kHz	40pF	40pF
	LXT1 (100K~1 MHz)	100kHz	60pF	60pF
		200kHz	60pF	60pF
		455kHz	40pF	40pF
		1 MHz	30pF	30pF
	XT (1~6 MHz)	455kHz	30pF	30pF
		1.0 MHz	30pF	30pF
		2.0 MHz	30pF	30pF
		4.0 MHz	20pF	20pF
		6.0 MHz	30pF	30pF
	HXT2 (6~12 MHz)	6.0 MHz	30pF	30pF
		8.0 MHz	20pF	20pF
		10.0 MHz	30pF	30pF
		12.0 MHz	30pF	30pF

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
	HXT1 (12~20 MHz)	12.0 MHz	30pF	30pF
		16.0 MHz	20pF	20pF
		20.0 MHz	15pF	15pF

Note: The values of Capacitors C1 and C2 are for reference only

6.7.3 Internal RC Oscillator Mode

EM79F701N offers a versatile internal RC mode with default frequency value of 4MHz. The Internal RC oscillator mode has other frequencies (1MHz, 8MHz, and 16MHz) that can be set by Code Option (Word 1), RCM1, and RCM0. The table below describes the EM79F701N internal RC drift with variation of voltage, temperature, and process.

Table 7 Internal RC Drift Rate (Ta=25°C, VDD=5V ± 5%, VSS=0V)

Internal RC Frequency	Drift Rate (NUWTR)			
	Temperature (-40°C~85°C)	Voltage	Process	Total
4 MHz	± 2.5%	± 3% @ 2.1V ~ 5.5V	± 0.5%	± 6%
16 MHz	± 2.5%	± 2% @ 4.0V ~ 5.5V	± 0.5%	± 5%
8 MHz	± 2.5%	± 2% @ 3.0V ~ 5.5V	± 0.5%	± 5%
1 MHz	± 2.5%	± 3% @ 2.1V ~ 5.5V	± 0.5%	± 6%

Internal RC Frequency	Drift Rate (UWTR)			
	Temperature (-40°C~85°C)	Voltage	Process	Total
4 MHz	± 2.5%	± 3% @ 2.1V ~ 5.5V	± 1.5%	± 7%
16 MHz	± 2.5%	± 2% @ 4.0V ~ 5.5V	± 1.5%	± 6%
8 MHz	± 2.5%	± 2% @ 3.0V ~ 5.5V	± 1.5%	± 6%
1 MHz	± 2.5%	± 3% @ 2.1V ~ 5.5V	± 1.5%	± 7%

Note: These are theoretical values provided for reference only. Actual values may vary depending on the actual process.

6.8 Code Option

The MCU has Code Option Words and one Customer ID word that are not part of the normal program memory.

6.8.1 Code Option (Word 0)

Word 0								
	Bit 15	Bit 14	Bit 13	Bit 12	Bit11	Bit10	Bit9	Bit8
Mnemonic				RESETEN	ENWDT	CLKS	LVR1	LVR0
0	Low	Low	Low	Enable	Enable	2 clocks	Low	Low
1	High	High	High	Disable	Disable	4 clocks	High	High
Default	1	1	1	1	1	1	1	1
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mnemonic		WDTPS1	WDTPS0	NRHL	NRE			
0	Low	Low	Low	8/fc	Disable	Low	Low	Low
1	High	High	High	32/fc	Enable	High	High	High
Default	1	1	1	1	1	1	1	1

Bit 12 (RESETEN): RESET/P63 Pin Select Bit

0: P63 set to /RESET pin

1: P63 is general purpose input pin or open-drain for output Port (default)

Bit 11 (ENWDT): Watchdog timer enable bit

0: Enable

1: Disable (default)

Bit 10 (CLKS): Instruction period option bit

0: two oscillator periods

1: four oscillator periods (default)

Bits 9~8 (LVR1 ~ LVR0): Low Voltage Reset enable bits.

LVR1, LVR0	VDD Reset Level	VDD Release Level
11	NA (Power-on Reset) (Default)	
10	2.7V	2.9V
01	3.5V	3.7V
00	4.0V	4.2V

Bits 6~5 (WDTPS1 ~ WDTPS0): WDT Time-out Period of device bits.

Table 8 WDT Time-out Period of Device Programming

WDTPS1	WDTPS0	*WDT Time-out Period
1	1	18 ms (Default)
1	0	4.5 ms
0	1	288 ms
0	0	72 ms

* These are theoretical values, provided for reference only

Bit 4 (NRHL): Noise rejection high/low pulses define bit. INT pin is falling edge trigger

0: Pulses equal to 8/fc at CLKS=2 clocks, or pulses equal to 16/fc at CLKS=4 clocks is regarded as signal

1: Pulses equal to 32/fc at CLKS=2 clocks, or pulses equal to 64/fc at CLKS=4 clocks is regarded as signal (default)

Bit 3 (NRE): Noise rejection enable

0: disable noise rejection

1: enable noise rejection (default)

The noise rejection circuit is always disabled in Low Crystal oscillator (LXT2) and green/idle/sleep mode.

6.8.2 Code Option (Word 1)

Word 1								
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit11**	**Bit10**	**Bit9**	**Bit8**
Mnemonic		**TYPE**		**HLP**				
0	*Low*	*10 Pin*	*Low*	*Low*	*Low*	*Low*	*Low*	*Low*
1	High	14 Pin	High	High	High	High	High	High
Default	1	1	1	1	1	1	1	1
	Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Mnemonic		**RCM1**	**RCM0**	**OSC3**	**OSC2**	**OSC1**	**OSC0**	**RCOUT**
0	Low	Low	Low	Low	Low	Low	Low	Open-drain
1	High	High	High	High	High	High	High	System-clock
Default	1	1	1	1	1	1	1	1

Bit 14 (TYPE): Type selection

TYPE	MCU Type	PIN Not Used
0	EM79F701N-10Pin	Port 50 / 51 / 52 / 53 are output low
1 (Default)	EM79F701N-14Pin	None

Bit 12 (HLP): Power consumption mode

0: Low power consumption mode, applies to operating frequency at 1 MHz or below 1 MHz

1: High power consumption mode, except Oscillator mode LXT2 or CPUS=0 (default)

Bits 6~5 (RCM1, RCM0): RC mode selection bits

RCM 1	RCM 0	Frequency (MHz)
1	1	4 (Default)
1	0	16
0	1	8
0	0	1

* Theoretical values, for reference only

Bits 4 ~ 1 (OSC3 ~ OSC0): Oscillator Mode Selection bits

Oscillator Modes	OSC3	OSC2	OSC1	OSC0
IRC (Internal RC oscillator mode); P64/RCOUT act as P64	0	0	0	X
IRC (Internal RC oscillator mode); P64/RCOUT act as P64	0	0	1	0
IRC (Internal RC oscillator mode); P64/RCOUT act as RCOUT	0	0	1	1
LXT1 (Frequency range of LXT1 mode is 100kHz ~1MHz)	0	1	0	0
HXT1 (Frequency range of HXT1 mode is 12 MHz~20 MHz)	0	1	0	1
LXT2 (Frequency range of LXT2 mode is 32.768kHz)	0	1	1	0
HXT2 (Frequency range of HXT2 mode is 6 MHz~12 MHz)	0	1	1	1
IRC (Internal RC oscillator mode); P64/RCOUT act as P64	1	0	X	X
IRC (Internal RC oscillator mode); P64/RCOUT act as P64	1	1	0	0
IRC (Internal RC oscillator mode); P64/RCOUT act as P64	1	1	0	1
IRC (Internal RC oscillator mode); P64/RCOUT act as P64	1	1	1	0
XT (Frequency range of XT mode is 6 MHz~1 MHz) (default)	1	1	1	1

Bit 0 (RCOUT): Instruction clock output enable bit in IRC mode.

0: RCOUT pin is open drain.

1: RCOUT pin output instruction clock. (default)

6.8.3 Code Option (Word 2)

Word 2								
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit11**	**Bit10**	**Bit9**	**Bit8**
Mnemonic	**-**	**-**	**-**	**-**	**SFS**		**ID9**	**ID8**
0	Low	Low	Low	Low	128KHz	Low	Low	Low
1	High	High	High	High	16KHz	High	High	High
Default	1	1	1	1	1	1	1	1
	Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Mnemonic	**ID7**	**ID6**	**ID5**	**ID4**	**ID3**	**ID2**	**ID1**	**ID0**
0	Low	Low	Low	Low	Low	Low	Low	Low
1	High	High	High	High	High	High	High	High
Default	1	1	1	1	1	1	1	1

Bit 11 (SFS): Sub Frequency Select for Green mode.

(Not included WDT time-out and POR release setup-up time)

0: 128kHz

1: 16kHz

Bits 9 ~ 0: Customer's ID9~0.

6.9 Power-on Consideration

No microcontroller can be guaranteed to start working properly until the power supply is stabilized in its steady state. Under customer application, when power is OFF, Vdd must drop below 1.8V and remain OFF for 10μs before power can be switched ON again. In this way, the EM79F701N will reset and operate normally. The extra external reset circuit will work well if Vdd can rise at very fast speed (50 ms or less). However, in most cases involving critical applications, extra devices are required to assist in solving the power-up issues.

6.10 Programmable Oscillator WDT Time-out Period

The Option word contains WDTPS0 and WDTPS1 which can be used to define the oscillator WDT time-out Period. Theoretically, the range is from 4.5 ms to 288 ms. For most of crystal or ceramic resonators, the lower the operation frequency is, the longer the Set-up time may be required.

6.11 External Power-on Reset Circuit

The circuit shown in Figure 6-15 implements an external RC to produce the reset pulse. The pulse width (time constant) should be kept long enough for Vdd to reach minimum operation voltage. This circuit is used when the power supply has a slow rise time.

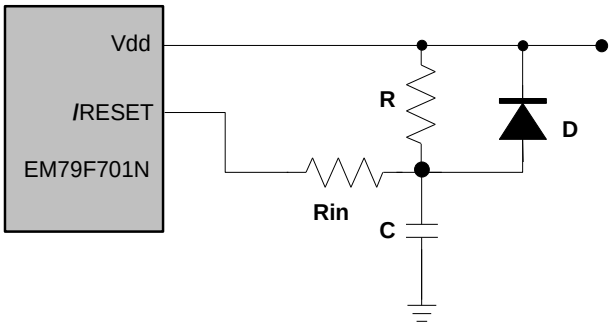


Fig 6-15 External Power-up Reset Circuit

Since the current leakage from the /RESET pin is ± 5μA, it is recommended that R should not be greater than 40K. In this way, the /RESET pin voltage is held below 0.2V. The diode (D) acts as a short circuit at the moment of power down. The capacitor C will discharge rapidly and fully. Rin, the current-limited resistor, will prevent high current or ESD (electrostatic discharge) from flowing to pin /RESET.

6.12 Residue-Voltage Protection

When the battery is replaced, the device power (Vdd) is cut off but residue-voltage remains. The residue-voltage may trip below the minimum Vdd, but not to zero. This condition may cause a poor power-on reset. The following figures illustrate two recommended methods on how to build a residue-voltage protection circuit for the EM79F701N.

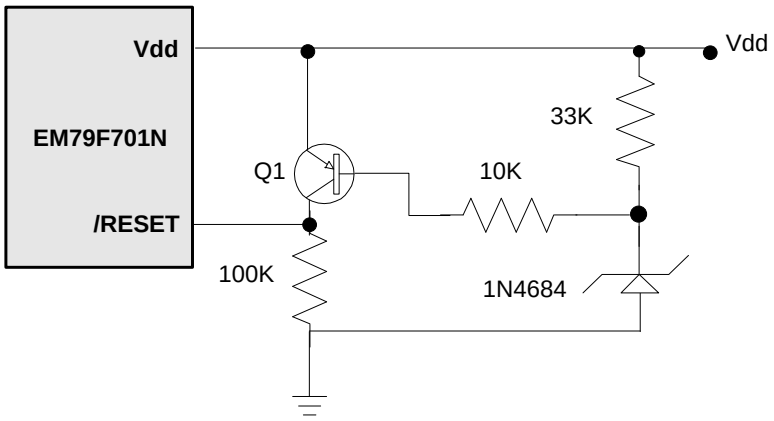


Figure 6-16 Residue Voltage Protection Circuit 1

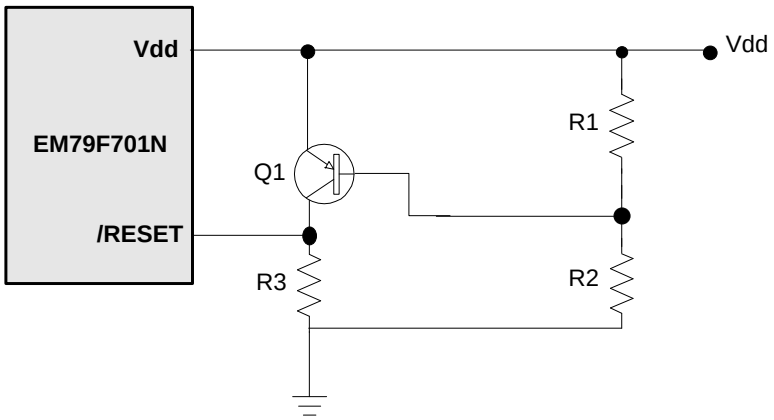


Figure 6-17 Residue Voltage Protection Circuit 2

NOTE

Figure 6-16 and Figure 6-17 should be designed to ensure that the voltage of the /RESET pin is larger than VIH (min).

6.13 Low Voltage Detector

When an unstable power source condition occurs, such as external power noise interference or EMS test condition, a violent power vibration is generated. At the same time, the Vdd becomes unstable as it could be operating below the working voltage. When the system supply voltage (Vdd) is below the operating voltage, the IC kernel will automatically keep all register status.

6.13.1 Low Voltage Reset (LVR)

LVR property is set at Bits 9 and 8 of Code Option Word 0. Detailed operation mode is as follows:

Word 0								
	Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit11**	**Bit10**	**Bit9**	**Bit8**
Mnemonic				**RESETEN**	**ENWDT**	**CLKS**	**LVR1**	**LVR0**
0	Low	Low	Low	Enable	Enable	2 clocks	Low	Low
1	High	High	High	Disable	Disable	4 clocks	High	High
Default	1	1	1	1	1	1	1	1
	Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Mnemonic		**WDTPS1**	**WDTPS0**	**NRHL**	**NRE**			
0	Low	Low	Low	8/fc	Disable	Low	Low	Low
1	High	High	High	32/fc	Enable	High	High	High
Default	1	1	1	1	1	1	1	1

Bits 9~8 (LVR1 ~ LVR0): Low Voltage Reset enable bits.

LVR1, LVR0	VDD Reset Level	VDD Release Level
11	NA (Power-on Reset) (Default)	
10	2.7V	2.9V
01	3.5V	3.7V
00	4.0V	4.2V

6.13.2 Low Voltage Detector (LVD)

LVD property is set and Register Bank 0-RE and Bank 1-RE. Detailed operation mode is as follows:

BANK0 RE ISR1/WUCR1(Interrupt Status 1 and Wake-up Control Register 1)

Bit Num	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	/LVD	LVDIF	-	-	-	-	-	LVDWE
Type	R	F	R	R	R	R	R	R/W

Bit 7 (/LVD): Low voltage Detector state.

When the VDD pin voltage is lower than LVD voltage interrupt level (selected by LVD1 and LVD0), this bit will be cleared.

0: Low voltage is detected

1: Low voltage is not detected or LVD function is disabled

Bit 6 (LVDIF): LVD Interrupt Flag bit.

0: No interrupt occurs

1: With interrupt request

Set when VDD drops slowly and crosses the detect point, reset to “0” by software

Bits 5 ~ 1: Not used. Set to “0” at all time.

Bit 0 (LVDWE): Low Voltage Detect wake-up.

0: Disable Low Voltage Detect wake-up

1: Enable Low Voltage Detect wake-up

When the Low Voltage Detect is used to enter an interrupt vector or to wake-up the IC from Sleep/Idle mode with the Low Voltage Detect running, the LVDWE bit must be set to “Enable.“

BANK1 RE LVDCR/WUCR2 (LVD Control and Wake-up Control Register 2)

Bit Num	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LVDIE	LVDEN	LVD1	LVD0	-	-	-	EXWE
Type	R/W	R/W	R/W	R/W	R	R	R	R/W

NOTE

- *BANK1 RE<7> register is both readable and writable*
- *Individual interrupt is enabled by setting its associated control bit in the BANK1 RE<7> to "1."*
- *Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Figure 6-10 (Interrupt Input Circuit) under Section 6.6 (Interrupt).*
- *After LVDEN bit is set, you must wait at least 40us to stabilize LVD. If you go to sleep immediately after setting LVDEN, LVD will not work normally.*

Bit 7 (LVDIE): Low voltage detector interrupt enable bit.

0 : Disable low voltagedetector function

1 : Enable low voltage detector function

Bit 6 (LVDEN): Low voltage detector enable bit

0 : Disable the Low voltage detector function

1 : Enable the Low voltage detector function

Bits 5~4 (LVD1~0): Low voltage detector level bits.

LVDEN	LVD1, LVD0	LVD Voltage Interrupt Level	/LVD
1	11	Vdd ≤ 2.2V	0
		Vdd > 2.2V	1
1	10	Vdd ≤ 3.3V	0
		Vdd > 3.3V	1
1	01	Vdd ≤ 4.0V	0
		Vdd > 4.0V	1
1	00	Vdd ≤ 4.5V	0
		Vdd > 4.5V	1
0	××	NA	1

NOTE

IF Vdd has crossover at LVD voltage in interrupt level as VDD varies, LVD interrupt will occur.

6.13.3 Programming Process

Follow these steps to obtain data from the LVD**:**

1. Write to the two bits (LVD1: LVD0) on the Bank 1-RE (LVDCR) register to define the LVD level.
2. Set the LVDWE bit, if the wake-up function is in use.
3. Set the LVDIE bit, if the interrupt function is in use.
4. Write “ENI” instruction, if the interrupt function is in use.
5. Set LVDEN bit to “1.”

6. Wait 40us for LVD stable time, and write “SLEP” instruction or Polling /LVD bit.
7. Clear the low voltage detector interrupt flag bit (LVDIF) when Low Voltage Detector interrupt occurred.

NOTE

■ *The internal LVD module uses an internal circuit, and when the code option is set to enable the LVD module, the current consumption will increase to about 30 μA.*

■ *During Sleep mode, the LVD module continues to operate. If the device voltage drops slowly and crosses the detection point, the LVDIF bit will be set and the device will wake up from Sleep mode. The LVD interrupt flag will remain set at priority status.*

■ *When the system resets, the LVD flag is cleared.*

The following figure shows the LVD module detection point in an external voltage condition.

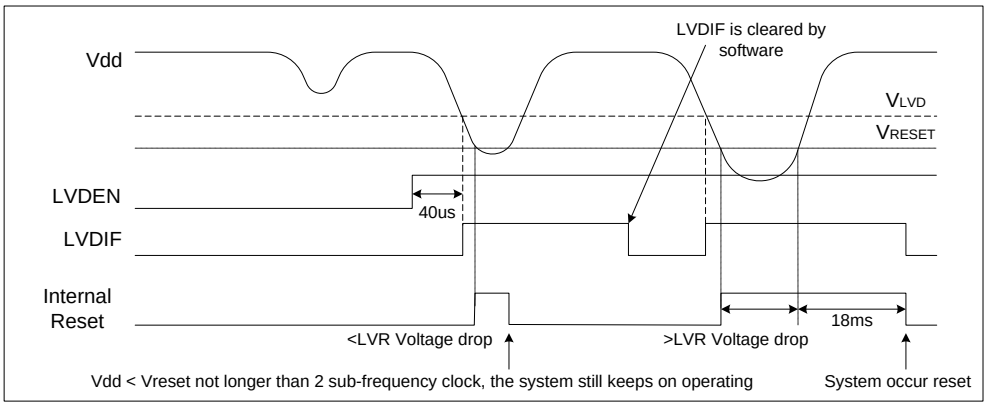


Figure 6-18 LVD/LVR Waveform with the Detection Point in an External Voltage Condition

- When the Vdd drops, but above V_{LVD}, the LVDIF is kept at **“0”**.
- When Vdd drops below V_{LVD}, the LVDIF is set to **“1”.** If global ENI is enabled, the LVDIF is also set to **“1”** and the next instruction will branch to an interrupt vector. The LVD interrupt flag is cleared to “0” by software.
- When Vdds drops below V_{RESET} at less than 2 sub-frequency clock, the system will keep all the registers’ status and halts it operation, but with the oscillation remaining active.
- When Vdd drops below V_{RESET} at more than 2 sub-frequency clock, a system reset will occur. Refer to Section 6.5.1, Reset for the detailed Reset description.

6.14 Instruction Set

Each instruction in the instruction set is a 15-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of two oscillator periods), unless the program counter is changed by instruction "MOV R2,A", "ADD R2,A", or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2,A", "BS(C) R2,6", "CLR R2", etc.). In this case, the execution takes two instruction cycles.

If for some reasons, the specification of the instruction cycle is not suitable for certain applications, try modifying the instruction as follows**:**

A) Modify one instruction cycle to consist of four oscillator periods.

B) "JMP", "CALL", "RET", "RETL", "RETI" or the conditional skip ("JBS", "JBC", "JZ", "JZA", "DJZ", "DJZA") commands which were tested to be true, are executed within one instruction cycle. The instructions that are written to the program counter also take one instruction cycle.

Case (A) is selected by the Code Option bit, called CLKS. One instruction cycle consists of two oscillator clocks if CLKS is low; and four oscillator clocks if CLKS is high.

Note that once the four oscillator periods within one instruction cycle is selected as in Case (A), the internal clock source to TCC should be CLKS=Fm/4, instead of Fm/2.

Moreover, the instruction set has the following features**:**

1) Every bit of any register can be set, cleared, or tested directly.
2) The I/O register can be regarded as general register. That is, the same instruction can operate on I/O register.

The following symbols are used in the Instruction Set table**:**

Convention:

R *= Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.*
Bit 6 in R4 determine the selected register bank.

b *= Bit field designator that selects the value for the bit located in the register* ***R*** *and which affects the operation.*

k *= 8 or 10-bit constant or literal value*

MNEMONIC	OPERATION	STATUS AFFECTED
NOP	No Operation	None
DAA	Decimal Adjust A	C
SLEP	0 → WDT, Stop oscillator	T,P
WDTC	0 → WDT	T,P
ENI	Enable Interrupt	None

MNEMONIC	OPERATION	STATUS AFFECTED
DISI	Disable Interrupt	None
RET	[Top of Stack] → PC	None [1]
RETI	[Top of Stack] → PC, Enable Interrupt	None [1]
MOV R,A	A → R	None
CLRA	0 → A	Z
CLR R	0 → R	Z
SUB A,R	R-A → A	Z,C,DC
SUB R,A	R-A → R	Z,C,DC
DECA R	R-1 → A	Z [3]
DEC R	R-1 → R	Z [3]
OR A,R	A ∨ R → A	Z
OR R,A	A ∨ R → R	Z
AND A,R	A & R → A	Z
AND R,A	A & R → R	Z
XOR A,R	A ⊕ R → A	Z
XOR R,A	A ⊕ R → R	Z
ADD A,R	A + R → A	Z,C,DC
ADD R,A	A + R → R	Z,C,DC
MOV A,R	R → A	Z
MOV R,R	R → R	Z
COMA R	/R → A	Z
COM R	/R → R	Z
INCA R	R+1 → A	Z [3]
INC R	R+1 → R	Z [3]
DJZA R	R-1 → A, skip if zero	None [1]
DJZ R	R-1 → R, skip if zero	None [1]
RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
RLCA R	R(n) → A(n+1),R(7) → C, C → A(0)	C
RLC R	R(n) → R(n+1),R(7) → C, C → R(0)	C
SWAPA R	R(0-3) → A(4-7),R(4-7) → A(0-3)	None
SWAP R	R(0-3) ↔ R(4-7)	None
JZA R	R+1 → A, skip if zero	None [1]
JZ R	R+1 → R, skip if zero	None [1]
BC R,b	0 → R(b)	None [4]
BS R,b	1 → R(b)	None [5]

MNEMONIC	OPERATION	STATUS AFFECTED
JBC R,b	if R(b)=0, skip	None [1]
JBS R,b	if R(b)=1, skip	None [1]
CALL k	PC+1 → [SP],, k → PC	None [1]
JMP k	k → PC	None [1]
MOV A,k	k → A	None
OR A,k	A ∨ k → A	Z
MOVX A,R	R → A	None
AND A,k	A & k → A	Z
XOR A,k	A ⊕ k → A	Z
RETL k	k → A,[Top of Stack] → PC	None [1]
SUB A,k	k-A → A	Z,C,DC
BANK k	k → R4(6)	None
TBRD R	If Bank 1 R5.7=0, machine code(7:0) → R Else Bank 1 R5.7 = 1, machine Code (14:8) → R(6:0), R(7)=(0)	None
ADD A,k	k+A → A	Z,C,DC

Note: [1] "JMP," "CALL," "RET," "RETL," "RETI," or the conditional skip ("JBS," "JBC," "JZ," "JZA," "DJZ," "DJZA") commands which were tested to be true, are executed within one instruction cycle.

[2] "INC," "INCA," "DEC," and "DECA" commands affect Z flag only.

[3] This instruction is not recommended for Bank 0 RF operation.

[4] This instruction cannot operate under Bank 0 RF.

7 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Input voltage	Vss-0.3V	to	Vdd+0.5V
Output voltage	Vss-0.3V	to	Vdd+0.5V
Working Voltage	2.1V	to	5.5V
Working Frequency	DC	to	20 MHz

8 DC Electrical Characteristics

Ta=25°C, VDD=5V, VSS=0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FXT	Crystal: VDD to 2.1V	Two cycles with two clocks	DC	-	4.0	MHz
	Crystal: VDD to 3V	Two cycles with two clocks	DC	-	8.0	MHz
	Crystal: VDD to 5V	Two cycles with two clocks	DC	-	20.0	MHz
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	-	-	±1	μA
VIH	Input High Voltage (VDD=5V)	P50~P53, P60~P67	2.0			V
VIL	Input Low Voltage (VDD=5V)	P50~P53, P60~P67			0.8	V
IOH1	Output High Voltage	VOH = 2.4V	-13.3	-19	-24.7	mA
IOL1	Low Sink Current (Ports 5 & 6)	VOL = 0.4V	11	17.5	22.75	mA
IOL2	Low Sink Current (P63)	VOL = 0.4V	15.75	22.5	29.25	mA
IPH	Pull-high current	Pull-high active, input pin at VSS	-50	-70	-90	μA
IPD	Pull-low current	Pull-low active, input pin at Vdd	20	40	60	μA
ISB1	Power down current	All input and I/O pins at VDD, output pin floating, WDT disabled	-	1	-	μA
ISB2	Power down current	All input and I/O pins at VDD, output pin floating, WDT enabled,	-	12	-	μA
ICC1	Operating supply current at two clocks	/RESET= 'High', Fm=32KHz (Crystal type,CLKS="0"), output pin floating, WDT disabled (VDD=3V)	-	12.5	-	μA
ICC2	Operating supply current at two clocks	/RESET= 'High', Fm=32KHz (Crystal type,CLKS="0"), output pin floating, WDT enabled (VDD=3V)	-	20	-	μA
ICC3	Operating supply current at two clocks	/RESET= 'High', Fm=4MHz (Crystal type, CLKS="0"), output pin floating, WDT enabled (VDD=5V)	-	3	-	mA

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
ICC4	Operating supply current at two clocks	/RESET= 'High', Fm=10MHz (Crystal type, CLKS="0"), output pin floating, WDT enabled (VDD=5V)	-	4.2	-	mA

NOTE

These parameters are theoretical values and have not been tested.

■ **Internal RC Electrical Characteristics (Ta=25°C, VDD=5 V, VSS=0V)**

Internal RC	Drift Rate (NUWTR)				
	Temperature	Voltage	Min.	Typ.	Max.
4 MHz	25°C	5V	3.98 MHz	4 MHz	4.02 MHz
16 MHz	25°C	5V	15.92 MHz	16 MHz	16.08 MHz
8 MHz	25°C	5V	7.96 MHz	8 MHz	8.04 MHz
1 MHz	25°C	5V	0.995MHz	1MHz	1.005MHz

■ **Internal RC Electrical Characteristics (Ta= -40 ~85°C)**

Internal RC	Drift Rate (NUWTR)				
	Temperature	Voltage	Min.	Typ.	Max.
4 MHz	-40 ~ 85°C	2.1V~5.5V	3.76 MHz	4 MHz	4.24 MHz
16 MHz	-40 ~ 85°C	4.0V~5.5V	15.36 MHz	16MHz	16.64 MHz
8 MHz	-40 ~ 85°C	3.0V~5.5V	7.60 MHz	8 MHz	8.40 MHz
1 MHz	-40 ~ 85°C	2.1V~5.5V	0.94 MHz	1MHz	1.06 MHz

9 AC Electrical Characteristics

Ta=25°C, VDD=5V ± 5%, VSS=0V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Dclk	Input CLK duty cycle	-	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100	-	DC	ns
		RC type	500	-	DC	ns
Ttcc	TCC input period	-	(Tins+20)/N*	-	-	ns
Tdrh	Device reset hold time	Ta = 25°C, Crystal, WDTPS1, WDTPS0=1,1	16.8-30%	16.8	16.8+30%	ms
Trst	/RESET pulse width	Ta = 25°C	2000	-	-	ns
*Twdt1	Watchdog timer period	Ta = 25°C WDTPS1, WDTPS0=1,1	16.8-30%	16.8	16.8+30%	ms
*Twdt2	Watchdog timer period	Ta = 25°C WDTPS1, WDTPS0=1,0	4.5-30%	4.5	4.5+30%	ms
*Twdt3	Watchdog timer period	Ta = 25°C WDTPS1, WDTPS0=0,1	288-30%	288	288+30%	ms
*Twdt4	Watchdog timer period	Ta = 25°C WDTPS1, WDTPS0=0,0	72-30%	72	72+30%	ms
Tset	Input pin setup time	-	-	0	-	ns
Thold	Input pin hold time	-	-	20	-	ns
Tdelay	Output pin delay time	Cload=20pF	-	50	-	ns

Note: These parameters are theoretical values and have not been tested.

The Watchdog Timer duration is determined by Code Option (Word0 Bit 6, Bit 5)

*N = selected prescaler ratio

*Twdt1: The Option word (WDTPS1, WDTPS0) is used to define the oscillator set-up time. In Crystal mode the WDT time-out length is the same as set-up time (18ms).

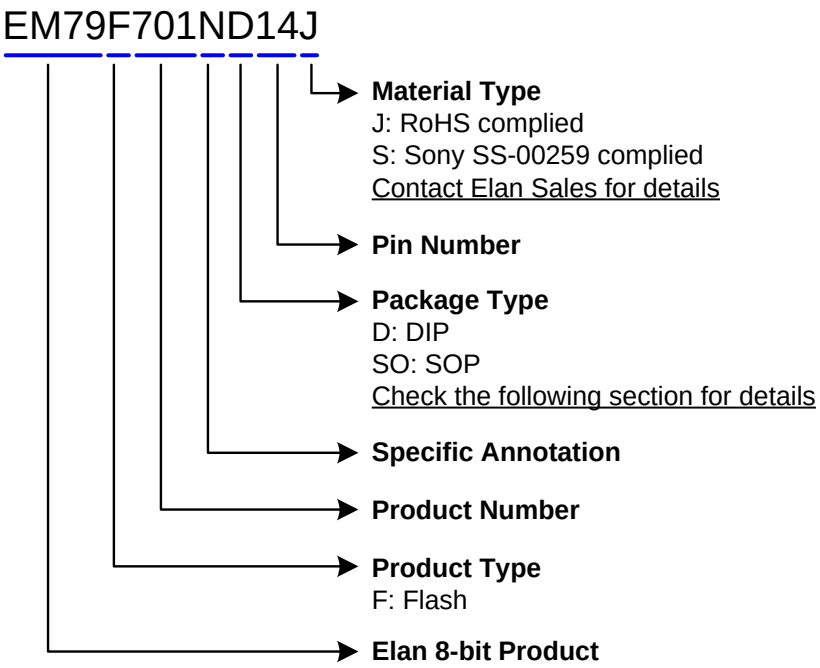
*Twdt2: The Option word (WDTPS1, WDTPS0) is used to define the oscillator set-up time. In Crystal mode the WDT time-out length is the same as set-up time (4.5ms).

*Twdt3: The Option word (WDTPS1, WDTPS0) is used to define the oscillator set-up time. In Crystal mode the WDT time-out length is the same as set-up time (288ms).

*Twdt4: The Option word (WDTPS1, WDTPS0) is used to define the oscillator set-up time. In Crystal mode the WDT time-out length is the same as set-up time (72ms).

APPENDIX

A Ordering and Manufacturing Information

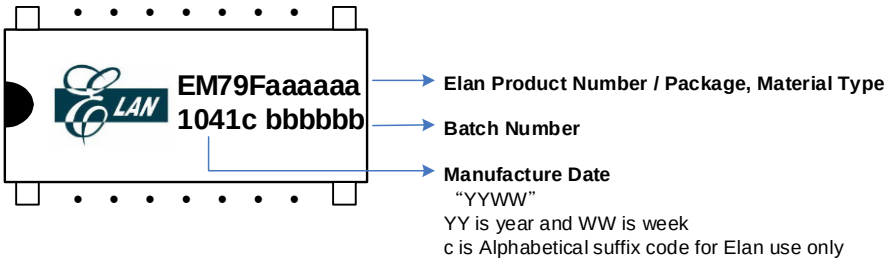


For example:

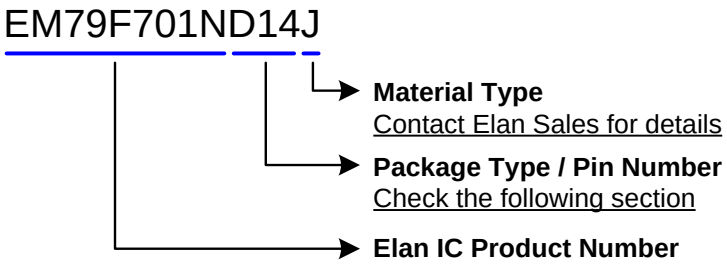
EM79F701NSO14S

is EM79F701N with Flash program memory, product,
in 14-pin SOP 150mil package with Sony SS-00259 complied

IC Mark



Ordering Code



B Package Type

Flash MCU	Package Type	Pin Count	Package Size
EM79F701ND14	DIP	14	300 mil
EM79F701NSO14	SOP	14	150 mil
EM79F701NMS10	MSOP	10	118 mil

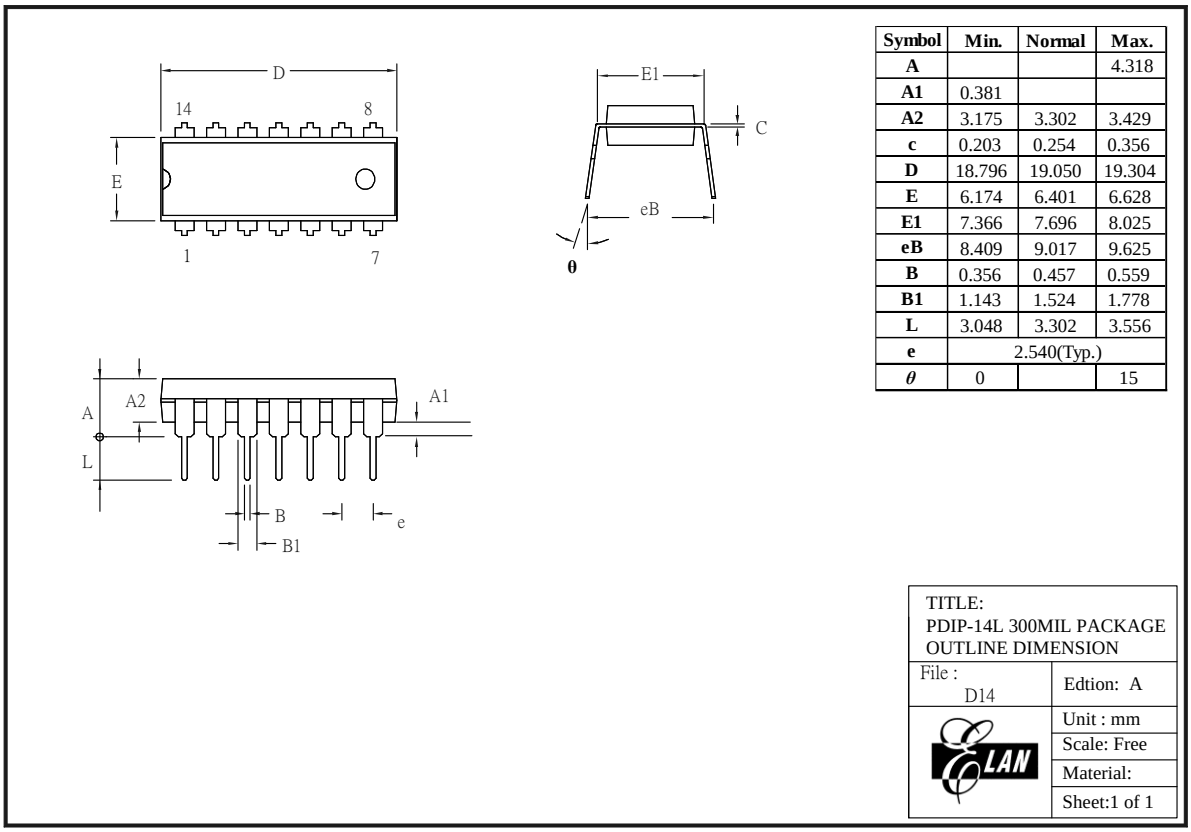
These are Green products which do not contain hazardous substances and comply with the third edition of Sony SS-00259 standard.

Pb content is less than 100ppm and complies with Sony specifications.

Part No.	EM79F701NxJ/xS
Electroplate type	Pure Tin
Ingredient (%)	Sn:100%
Melting point (°C)	232°C
Electrical resistivity (μΩ-cm)	11.4
Hardness (hv)	8~10
Elongation (%)	>50%

C Package Information

■ 14-Lead Plastic Dual In–line Package (PDIP) — 300 mil

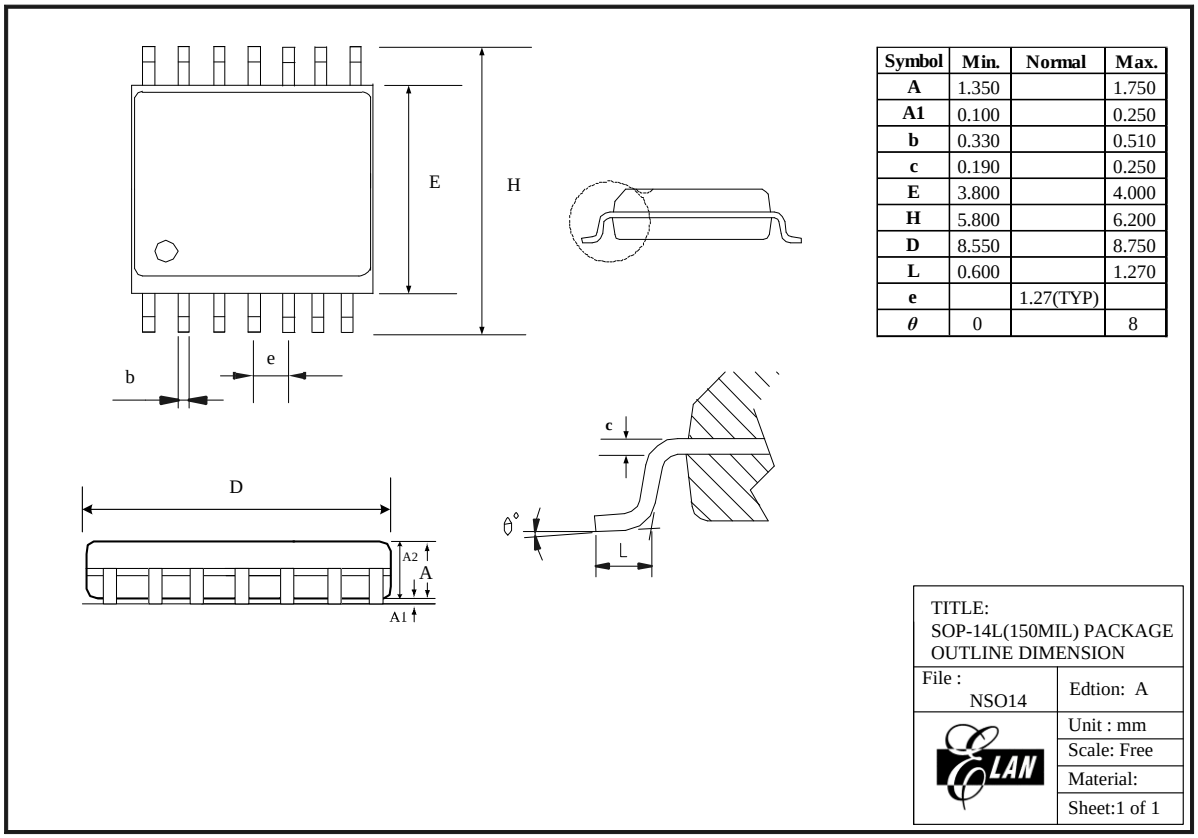


Symbol	Min.	Normal	Max.
A			4.318
A1	0.381		
A2	3.175	3.302	3.429
c	0.203	0.254	0.356
D	18.796	19.050	19.304
E	6.174	6.401	6.628
E1	7.366	7.696	8.025
eB	8.409	9.017	9.625
B	0.356	0.457	0.559
B1	1.143	1.524	1.778
L	3.048	3.302	3.556
e	2.540(Typ.)		
θ	0		15

TITLE: PDIP-14L 300MIL PACKAGE OUTLINE DIMENSION	
File : D14	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure C-1a EM79F701N 14-Lead PDIP Package Type

■ 14-Lead Small Outline Package (SOP) — 150 mil

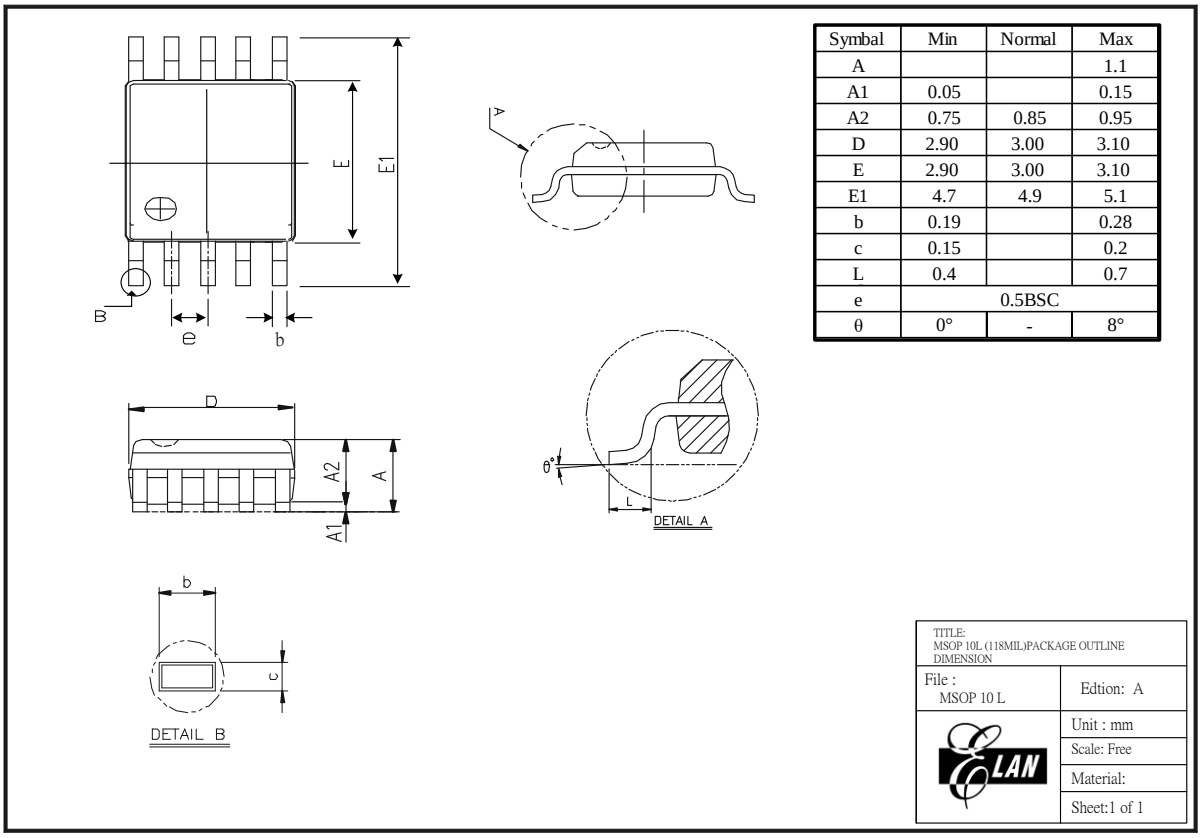


Symbol	Min.	Normal	Max.
A	1.350		1.750
A1	0.100		0.250
b	0.330		0.510
c	0.190		0.250
E	3.800		4.000
H	5.800		6.200
D	8.550		8.750
L	0.600		1.270
e		1.27(TYP)	
θ	0		8

TITLE: SOP-14L(150MIL) PACKAGE OUTLINE DIMENSION	
File : NSO14	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

Figure C-1b EM79F701N 14-Lead SOP Package Type

■ ***10-Lead Micro Small Outline Package (MSOP) — 118 mil***



Symbal	Min	Normal	Max
A			1.1
A1	0.05		0.15
A2	0.75	0.85	0.95
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E1	4.7	4.9	5.1
b	0.19		0.28
c	0.15		0.2
L	0.4		0.7
e	0.5BSC		
θ	0°	-	8°

Figure C-1c EM79F701N 10-Lead MSOP Package Type

D Writer Connection

- **Connecting NUWTR to Host Computer and Power Source**

Figure D-1 Connecting NUWTR Writer to Host Computer (Left / Top / Right View)

- **Program Interface: Socket**

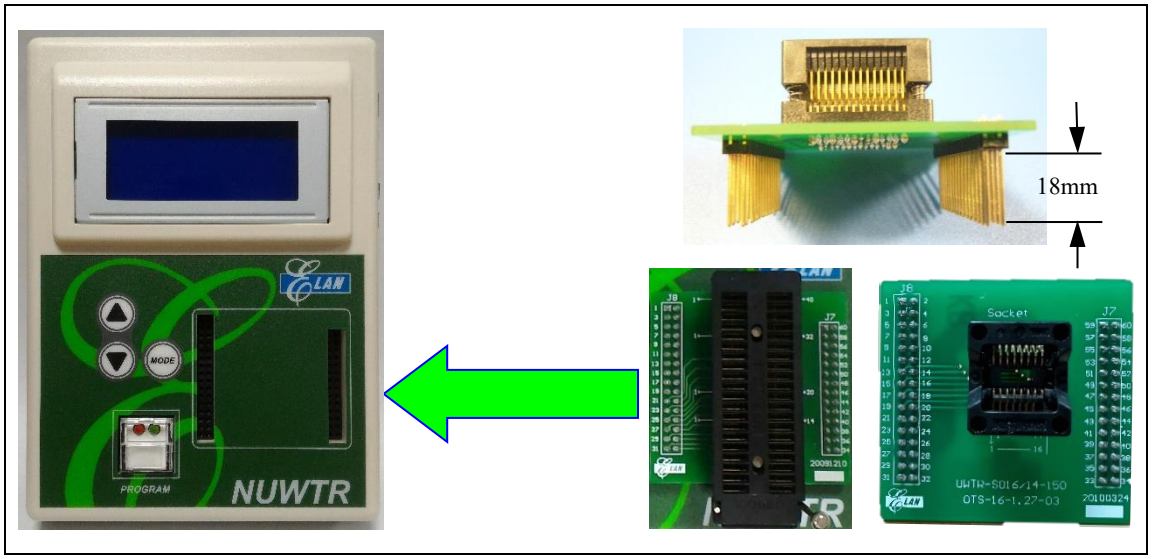
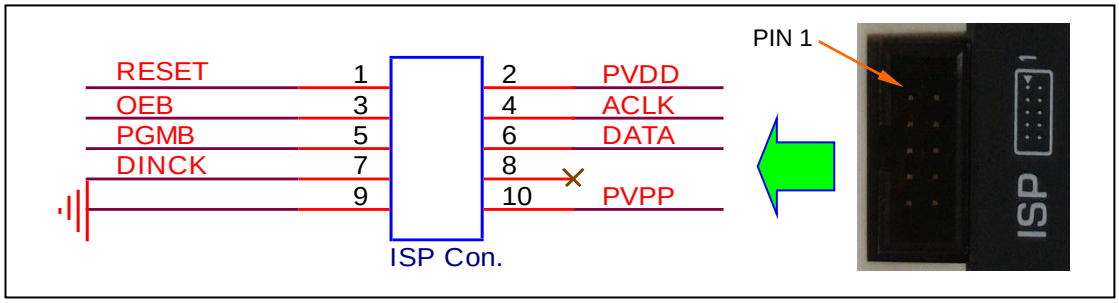


Figure D-2 Mounting Textool (with Pin Height of 18 mm) on NUWTR Writer

■ **Program Interface: ISP**



Applicable pins for EM79F701N**:**

1: RESET **2:** PVDD **6:** DATA **7:** DINCK **9:** GND **10:** PVPP

Figure D-3 In-System-Programming (ISP) Connector Pin Assignments

When VPP pulls to 11V, the system will be in programming mode. The Writer can program the code ROM inside the system.

IC Pin No.	System Pin Name	Writer Pin Name	Description
4	VDD	VDD	VDD power
7	P63	PVPP	High voltage activation pin for programming
9	P61	DINCK	On Chip Program clock pin
10	P60	DATA	On Chip Program data pin
11	VSS	GND	Ground power

NOTE

When programming EM79F701N, Writer will supply 5V to VDD and supply max 11.2V to VPP (RESET PIN). Therefore, during EM79F701N programming, pay attention to the voltage rating of the surrounding components.